Snell & Wilcox

MDE 1000

Multi-Standard Digital Encoder

Operator's Manual

SNELL & WILCOX LTD
DURFORD MILL, PETERSFIELD, HANTS. GU31 5AZ UNITED KINGDOM

Safety Warnings

Always ensure that the unit is properly earthed and power connections correctly made.

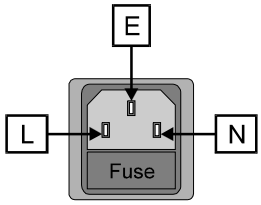
This equipment shall be supplied from a power system providing a protective earth connection and having an earthed neutral which can be reliably identified.

The power terminals of the IEC mains input connector are identified as shown below:

E = Protective Earth Conductor

N = Earthed Neutral Conductor

L = Phase Conductor



The equipment is normally shipped with a power cable with a standard IEC moulded free socket on one end and unterminated conductors on the other. If this cable is used the colour coded conductors should be connected as follows:

GREEN/YELLOW lead connected to E (Protective Earth Conductor)

BLUE lead connected to N (Earthed Neutral Conductor)

BROWN lead connected to L (Phase Conductor)

Warnings

Voltages within this unit can be lethal under certain circumstances. Where power is required to be connected to the unit during servicing great care must be taken to avoid contact with these voltages.

Maintenance should only be carried out by suitably qualified personnel.

EMC Standards

This unit has been designed to conform to the following standards:

Electromagnetic Compatibility-Generic Immunity Standard BS EN 50082-1:1992

The European Standard EN 50082-1:1992 has the status of a British Standard and is related to European Council Directive 89/336/EEC dated 3rd May 1989.

Electromagnetic Compatibility-Generic Emission Standard BS EN 50081-1:1992

The European Standard EN 50081-1:1992 has the status of a British Standard and is related to European Council Directive 89/336/EEC dated 3rd May 1989.

Safety Standards

This unit conforms to EN60950:1992 as ammended by ammendment A1(May 1993) and ammendment A2(March 1994). Specification for safety of technology equipment, including electrical business equipment.

EMC Performance of Cables and Connectors

Snell & Wilcox products are designed to meet or exceed the requirements of the appropriate European EMC standards. In order to achieve this performance in real installations it is essential to use cables and connectors with good EMC characteristics.

All signal connections (including remote control connections) shall be made with screened cables terminated in connectors having a metal shell. The cable screen shall have a large-area contact with the metal shell.

COAXIAL CABLES

Coaxial cables connections (particularly serial digital video connections) shall be made with high-quality double-screened coaxial cables such as Belden 8281 or BBC type PSF1/2M.

D-TYPE CONNECTORS

Table of Contents

Packing List

This unit is supplied in dedicated packing carton provided by the manufacturer and should not be accepted if delivered in inferior or unauthorised materials.

Carefully unpack the carton and check for any shipping damage.

Check against the following list for any shortages or damage and report any shortages or damage to the supplier **immediately.**

*Shipping Damage

*MDE1000 Multi-Standard Digital Encoder unit

*Power Cable

*Operators Manual

Manual Revision Record

Date	Version No.	Issue No.	Change	Comments
270397	1	2	pages 3.5, 3.6	SW2 8,9 function defined
111197	1	3	Page 3.5, line 23 data added Page 3.8 VITS Position added	New section 0 and 3 issued

Description

The MDE1000 is a digital encoder designed to encode 10 bit component digital video into any of the worlds major composite standards.
Providing outputs of PAL NTSC SECAM PALM and PALN the encoding process is entirely digital needing no setup or maintenance.
The unit is housed in a compact 1U X 19 inch rack frame, and contains the switched mode power supply, axial blower for cooling and two PCBs (the AOP and IPD) for video processing.

The IPD 'input digital' PCB performs decoding of the input component digital video signal which can be either parallel or serial format. The system microcomputer is also contained on the PCB together with all user controls.

Luminance from the input can be processed by the digital notch filter,and this provides ten levels of non linear attenuation of those signal components located around the output subcarrier frequency which could give rise to annoying cross effects when the output is decoded. This PCB also has a frame memory giving the unit a delay of one frame with respect to the reference input.

The output of the IPD PCB is 10 bits of luminance at 13.5MHz and 10 bits of Cb and Cr at 6.75MHz with timing and preprocessing applied, this signal is passed to the AOP PCB together with video timing information.

The AOP PCB performs the digital encoding function. All functions necessary for encoding to take place are contained on this PCB, including subcarrier generation, chrominance filtering and level transcoding.
Blanking and the addition of the composite timing information are also performed on this PCB.

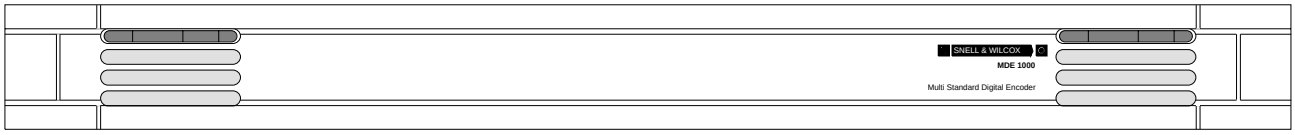
The encoded digital output is rounded to 12 bits and converted to an analogue signal using a high speed 12 bit D to A converter. This signal is filtered by a high quality 5.75MHz filter, and buffered to drive up to 5 outputs.

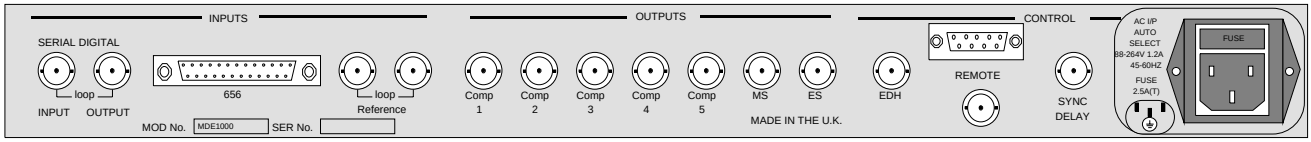
General Method of Operation

All user controls are located on the front edge of the IPD PCB this is the bottom PCB within the MDE1000 mainframe. The user controls comprise 2 rotary hex switches, 2 push buttons and 8 toggle (DIL) switches listed left to right and a block of 32 toggle (DIL) switches at the card right. There are 12 LED indicators showing status.

Features

- ☐ The best quality bridge from 4:2:2 to composite.
- ☐ 10 bit fully digital encoding process.
- ☐ Full support for EDH (SMPTE 165).
- ☐ All major world composite standards, PAL, NTSC, SECAM, PALM & PALN.
- ☐ Luminance channel processed by unique digital notch.
- ☐ Unit delay of 1 frame for easy system integration.
- ☐ Built in comprehensive 10 bit test signal generator.
- ☐ Digital 10 bit VITS inserter.
- ☐ Outputs are derived from a 12 bit D to A converter.
- ☐ Switchable serial and parallel 4:2:2 inputs.
- ☐ Automatic 525 625 input detection.
- ☐ Automatic reference standard detection.
- ☐ Delay output flag.
- ☐ Compact 1U X 19 inch format.





Specifications

PERFORMANCE

Frequency response	5.75MHz better than +0 -0.25dB.
U channel frequency response	-3dB @ 1.3 MHz.
V channel frequency response	-3dB @ 1.3 MHz.
I channel frequency response	-3dB @ 1.3 MHz.
Q channel frequency response	-3dB @ 600 KHz.
Q wide band channel frequency response	-3dB @ 1.3 MHz.
DC component on output	<±50mV.
Differential phase error	<0.5 degree of subcarrier.
Differential gain error	<0.5 %.
Luminance to chrominance timing error	Less than 10ns.
Luminance K Factor 2T pulse	<0.5%.
Weighted signal to noise ratio	>60 dB.
NTSC setup	54mV.
Subcarrier on output (no colour difference input)	0mV.
Sch Phase	Nominal value 0 degree. (Can be set by user to 1 degree accuracy)
Electrical path length	Can be set to 1 line or 1 frame.
Luminance notch depth	Can be set between 0 and 100% at Fsc.
Default notch depth	40%.
Subcarrier jitter wrt reference input in subcarrier lock	±0.5 degree.
Subcarrier jitter wrt reference input in line lock	±1.0 degree.

FRONT PANEL CONTROLS

None

CONTROL SYSTEM

1. By use of card edge controls located behind the drop-down front panel
2. By RS422 via rear mounted 9 pin D connector
3. By use of Snell & Wilcox net*

*The ‘Snell & Wilcox net’ is a specially designed remote control network system.
Full protocol documentation is available on request from Snell & Wilcox Ltd.

Specifications

INPUTS SIGNALS

Parallel component video	Via a 25 way D type socket with pin-out in accordance with CCIR Rec 656. The input is terminated with 11 X 100 ohm resistive loads and should be encoded in accordance with CCIR Rec 601, 4:2:2 format.
Serial component video	An active loop-through input via BNC connectors. The input signal must be connected to the INPUT connector , where it is internally terminated in 75 Ohms, and the output signal taken from the OUTPUT connector. The serial input should be of scrambled format following the polynomial $(X^9+X^4+1)(X+1)$. This input contains an automatic equaliser allowing input lengths up to 200m when high quality coax is used. Return loss is better then 15dB.
Analogue reference	Passive loop-through with return loss greater then 35dB. 2 X BNC socket Reference signal is nominally of composite format 1Vpp or black & burst and the unit can operate with variations of +3dB and -3dB about this level. A mono source can also be used as reference but in this mode the unit will line lock rather than the subcarrier lock which is performed when a burst is present. When no reference is present the unit will perform line lock to the F and H data contained in the incoming video data.

OUTPUTS SIGNALS

Composite video	Five isolated outputs 1Vp-p via BNC connectors for 75 ohms and conforms to CCIR report 624-3. Return loss better then 35dB DC to 5.5 MHz.
Mixed sync	2Vp-p via BNC connector for 75 ohms
Early sync	2Vp-p via BNC connector for 75 ohms
Sync Delay	TTL signal representing the synchroniser delay time. Signal will go high at the beginning of input field 1, will stay high for the delay time and then go low at the end of the delay time. Maximum delay is 1 frame and increments in steps of 74ns. For use with auto-tracking audio delay units.

POWER REQUIREMENTS

Voltage Range	88V to 264V AC 1.2A 45Hz to 60Hz IEC320 inlet socket Fused 2.5A(T)
Power Consumption	40VA maximum.

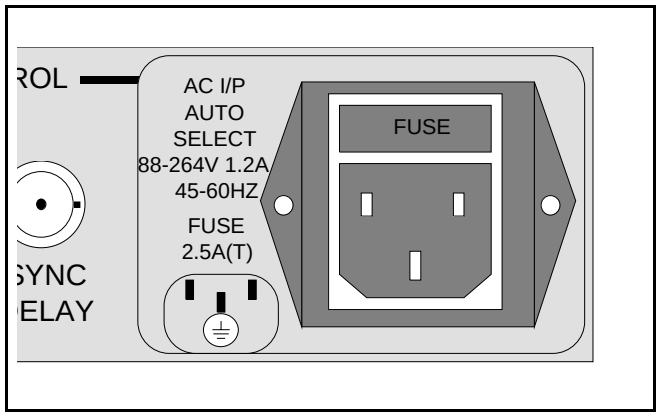
TEMPERATURE RANGE	0 to 40°C Operating, -30 to +75°storage
MECHANICAL	The unit is ruggedly constructed in a 19" 1U steel rack mount case
Dimensions	483mm X 495mm X 45mm (W,D,H)
Weight	10kg

Operation

POWER CONNECTIONS

This is the mains power connector suitable for a standard IEC type power cable and contains a 2.5A(T) fuse. If a fused plug is fitted to the cable a fuse of 7A Fast should be installed.

The power ON/OFF switch is located behind the drop down front panel in the left hand corner.



POWER INDICATOR

The front panel indicator lamp will glow:
GREEN-Under normal conditions
RED -If an EDH error is detected in last second
-If the cooling fan has failed

INPUT CONNECTIONS

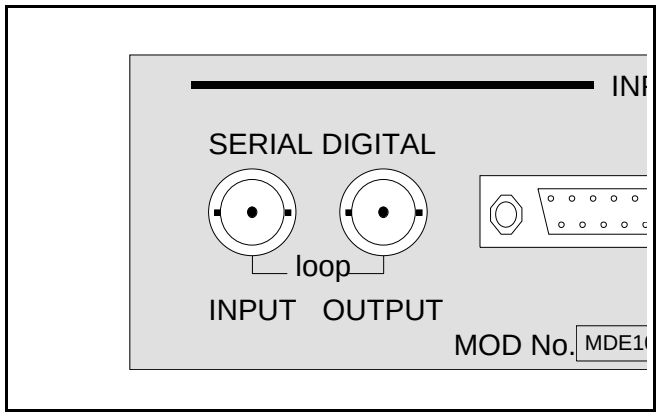
SERIAL DIGITAL INPUT

This is the Serial Digital input for the unit via BNC connectors.

As the loop-through is an active type, the input signal must be connected to the connector marked INPUT and is internally terminated in 75 Ohms.

Return loss is >15dB and input cable lengths of up to 200m may be used.

The OUTPUT connector provides a buffered output of the input signal.

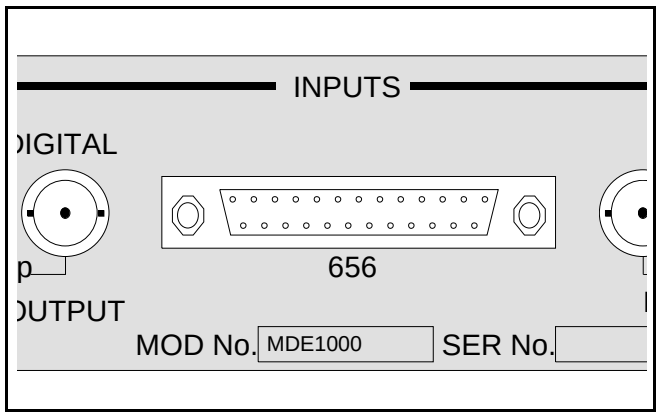


PARALLEL DIGITAL INPUT

This is the Parallel Digital input for the unit via a 25-way 'D' female connector.

The pin-out is in accordance with CCIR Rec. 656 and signal lines (11)are internally terminated in 100 Ohms.

The signal should be encoded in accordance with CCIR Rec. 601, 4:2:2 format.



Operation

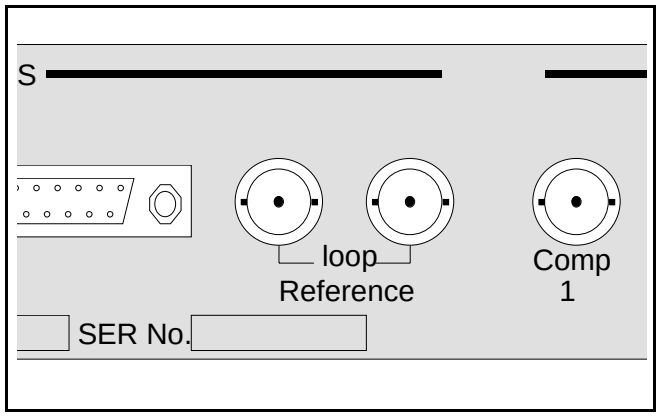
REFERENCE INPUT

When a suitable signal is connected to this connector, the unit, and the output signals, will be synchronised to this signal.

The signal may be black burst or standard composite colour video. A monochrome signal may be used as a reference signal but the unit will then line lock rather than subcarrier lock.

A passive loop-through connection is provided via BNC connectors and has a return loss of >35dB when correctly terminated with a 75 Ohm load.

When no reference is connected the unit will perform line lock to the F and H Data contained in any selected incoming video data.

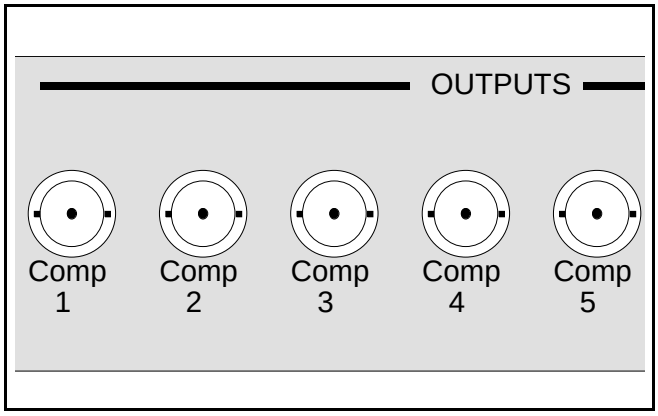


OUTPUT CONNECTIONS

COMPOSITE OUTPUTS

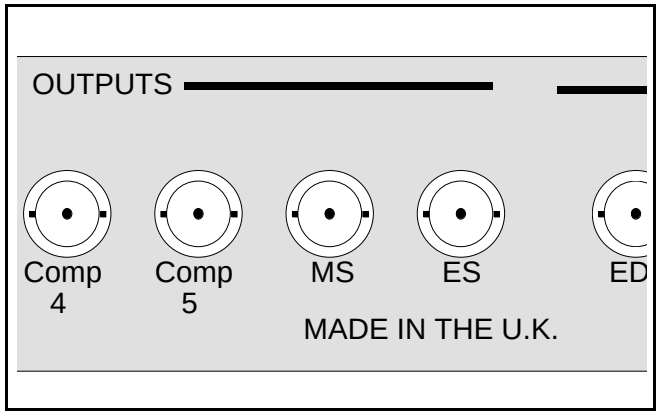
There are 5 isolated outputs of composite video available from the unit via BNC connectors.

Nominal output level is 1V p-p into 75 Ohms and Return Loss is >35dB to 5.5MHz.



MIXED SYNC OUTPUT (MS)

Mixed sync pulses are available from this BNC connector with a nominal level of 2V p-p into 75 Ohms.

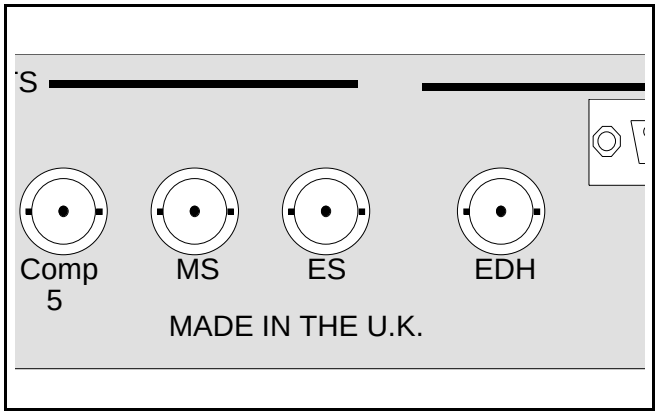


Operation

EARLY SYNC (ES)

Early sync pulses are available from this BNC connector with a nominal level of 2V p-p into 75 Ohms.

These syncs are in advance of the normal mixed syncs by a fixed amount of 2 lines.

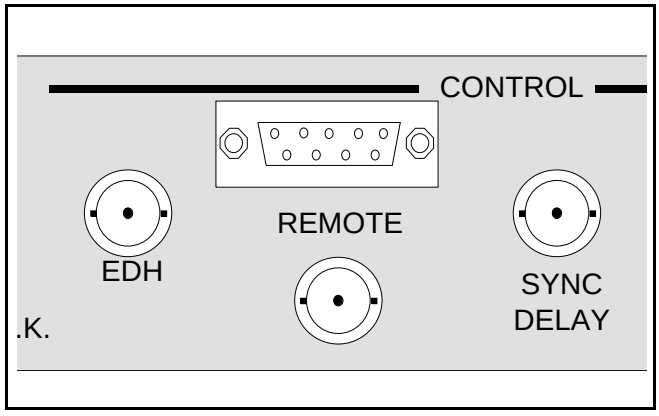


CONTROL

EDH

This connector provides an output from an opto-isolated open collector switch for reporting of EDH errors.

For details of the EDH system, see Section 4, Appendix 1.

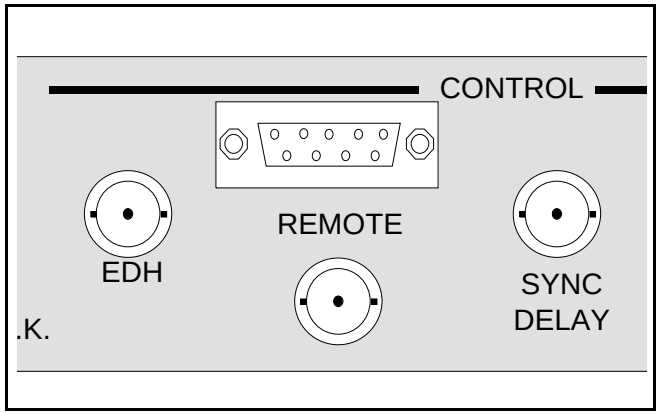


REMOTE

The RS 422 remote control interface is via this 9-pin female 'D' connector.

Interface with the S & W network is via the single BNC connector. Connections should be made by means of a 'T' piece (Zo=75Ohms) to a 75 Ohm cable system in a similar manner to a computer 'Ethernet' system. It should be noted that both extremities of the cable system must be terminated i 75 Ohms.

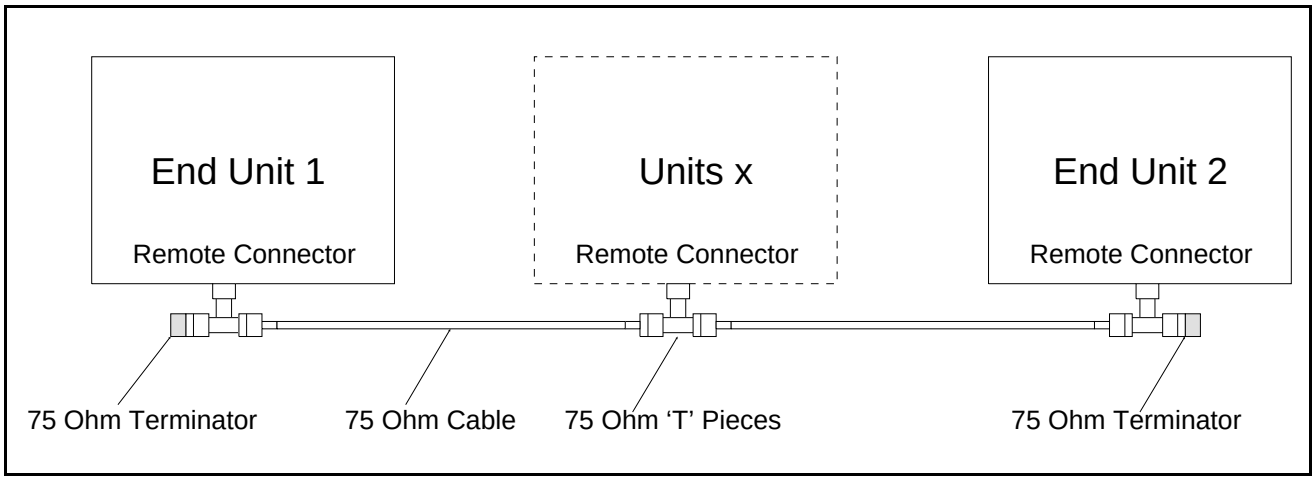
The 'Snell & Wilcox network' is a specially designed remote control network system.
Full protocol documentation is available on request from Snell & Wilcox Ltd.



Operation

REMOTE-MULTIPLE UNIT CONNECTIONS

Units should be connected together as shown below:



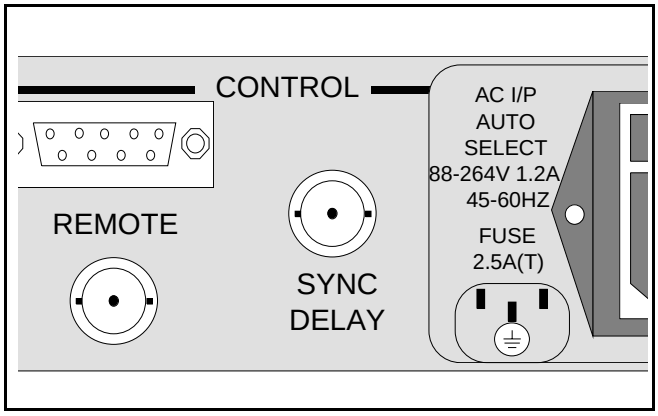
SYNC DELAY (Synchroniser Delay)

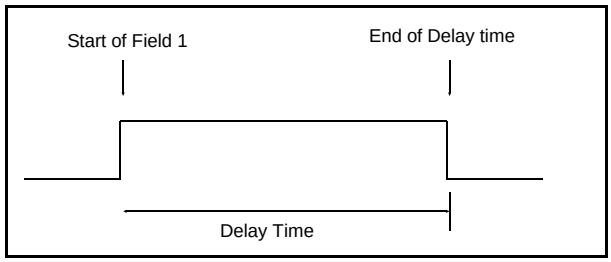
(For use with auto-tracking audio delay units)

This connector provides a TTL compatible signal representing the signal delay through the unit (synchroniser delay).

The signal will go high at the beginning of input field 1, stays high during the delay time, and then goes low at the end of the delay time.

The maximum delay time is 1 frame and the delay time increments in steps of 74ns.





Operation

GENERAL MODE OF OPERATION

All user controls are located on the front edge of the lower PCB within the MDE1000 mainframe.

The user controls comprise 2 rotary HEX switches, 2 push buttons and 8 toggle (DIL) switches and a block of 32 (4 X 8) toggle (DIL) switches.

There are also 12 LED indicators showing the status of various functions.

The HEX switch SW1 allows the standard of the output signal to be set.

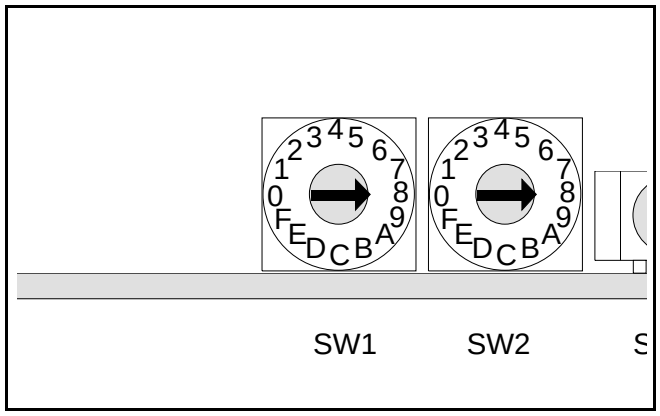
The two push button switches allow various parameters, selected by the HEX switch SW2, to be changed from their default settings. SW4 steps down through an invisible menu each time it is pressed (-) and SW5 steps up through an invisible menu each time it is pressed (+)
These settings may be stored in a non-volatile memory using SW2 and the push buttons. There are two memory locations available.

The 8-way DIL switch SW6 allows particular parameters to be set.

The bank of four 8-way DIL switches SW3, SW7 ,SW8 and SW9 allow particular lines of the input signal to be either blanked or passed (luminance only) through the the unit. Note that the notch function (set by SW6) will have no effect on lines passed through.

HEX SWITCH SW1

This switch selects the output standard of the encoded video signal generated.

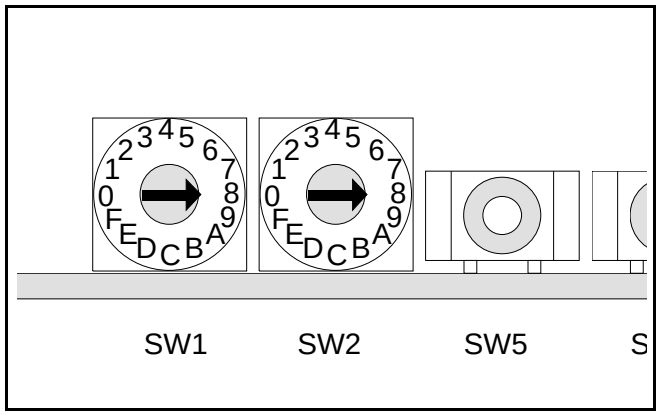


Position	Standard
0	Auto, output as reference. If no reference is connected the unit will output as follows: PAL if input is 625/D1 NTSC if input is 525/D1 Last valid standard if no input is connected.
1	Force PAL
2	Force NTSC
3	Force SECAM
4	Force PAL-M
5	Force PAL-N
6	AUTO +Force H-LOCK (Test Mode)
7	Function not defined
8	Force SECAM output with no subcarrier *Note that this setting should only be used for test purposes; use the default setting under any other circumstances.*
9	Allows line 23 (in PAL mode) to pass through the unit

Operation

HEX SWITCH SW2

This switch selects which function the push-buttons SW4 and SW5 will perform.

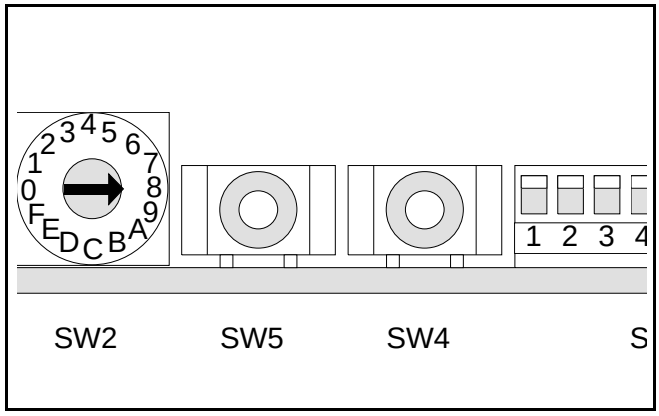


Position	Push Button Function
0	Chroma to Luma delay adjustment
1	Sets picture horizontal position
2	Sets depth of notch filter
3	Selects test signal
4	Sets subcarrier to horizontal sync phasing (Sch)
5	Sets output Subcarrier phase relative to reference input signal
6	Sets output H phase relative to reference input signal
7	Sets output V phase relative to reference input signal
8	SECAM Bottles ON/OFF
9	Sets SECAM depth of notch *Note that this setting should only be used for test purposes; use the default setting under any other circumstances.*
A	VITS position
B	Recalls set-up from memory
C	Saves set-up to memory
D	Return to factory defaults (press SW4 and SW5 together)
E	Reset EDH error log
F	Function not defined

Operation

PUSH BUTTON SWITCHES SW4 &SW5

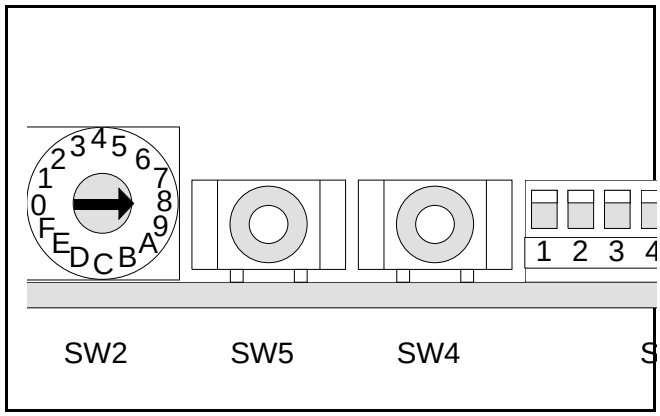
These switches control parameters, as selected by HEX switch SW2, to be changed and stored.
All settings, except D and E, have a default setting which may be recalled by pressing both buttons together.
SW4 steps down through an invisible menu each time it is pressed (-) and SW5 steps up through an invisible menu each time it is pressed (+)
These settings may be stored in a non-volatile memory using SW2. There are two memory locations available.



Details for each parameter are as follows:

Position	Parameter	Details
0	Y/C timing	Moves chroma signal relative to luma signal. Range is ±1.7us in 148ns steps. Default is zero relative delay.
1	Horizontal picture position	Range is ±888ns in 148ns steps.
2	Notch depth	10 steps of non-linear Y filter centred on system subcarrier. Default value is 40%. Note effect will only be apparent if 'NOTCH' is selected on DIL switch SW6.
3	Selects one of 13 test waveforms.	Waveforms available: Colour Bars 100% Colour Bars SMPTE (Top Group) in 525 standard. EBU Colour Bars in 625 standard. Y ramp, 10 bit C Wedge, 10 bit Black Y line sweep, 0.5MHz to 5.75MHz Cr multiburst (8 bit file) Cb multiburst (8 bit file) VITS signal 17, full field VITS signal 18, full field VITS signal 330, full field VITS signal 331, full field Legal ramps NOTE: Default is colour bars 100%

Operation



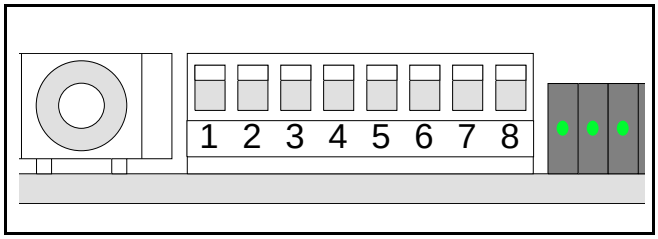
PUSH BUTTON SWITCHES SW4 & SW5 (cont)

Position	Parameter	Details
4	Set subcarrier to sync phasing (Sch).	Default is 0.
5	Set subcarrier phase relative to reference, when unit is subcarrier locked.	Increments in approximately one degree steps.
6	Set H phasing of output relative to reference.	SW4 (-ve) delays output, to a maximum of 10.4us. SW5 (+ve) advances output, to a maximum of 13us Increments in 74ns steps. Default is in phase.
7	Set V phasing of output relative to reference. Delay function (SW6) must be enabled to set this parameter.	SW4 (-ve) shifts the output sync earlier SW5 (+ve) shifts the output sync later Increments in 1 line steps. Default is 1 line delayed NOTE: Input data is NOT retimed with this shift.
8	Set SECAM Bottles ON or OFF	SW4 (-ve) sets bottles ON (default), (+ve) sets to OFF
9	SECAM Depth of Notch	8 steps of non-linear Y filter centred on system subcarrier
A	VITS Position	Alows the position of the VITS to be changed
B	Recall setting from memory	SW4 (-ve) will recall settings from memory location 1 SW5 (+ve) will recall settings from memory location 2
C	Save setup to memory	SW4 (-ve) will save to memory location 1 SW5 (+ve) will save to memory location 2
D	Clear Memory	SW4 and SW5 pressed together will clear all user settings and memories and revert to default values.
E	Clear EDH error log	SW4 and SW5 pressed together will clear EDH error log.
F	Function not defined	

Operation

8-WAY DIL SWITCH SW6

This switch array allows particular parameters and functions to be selected.



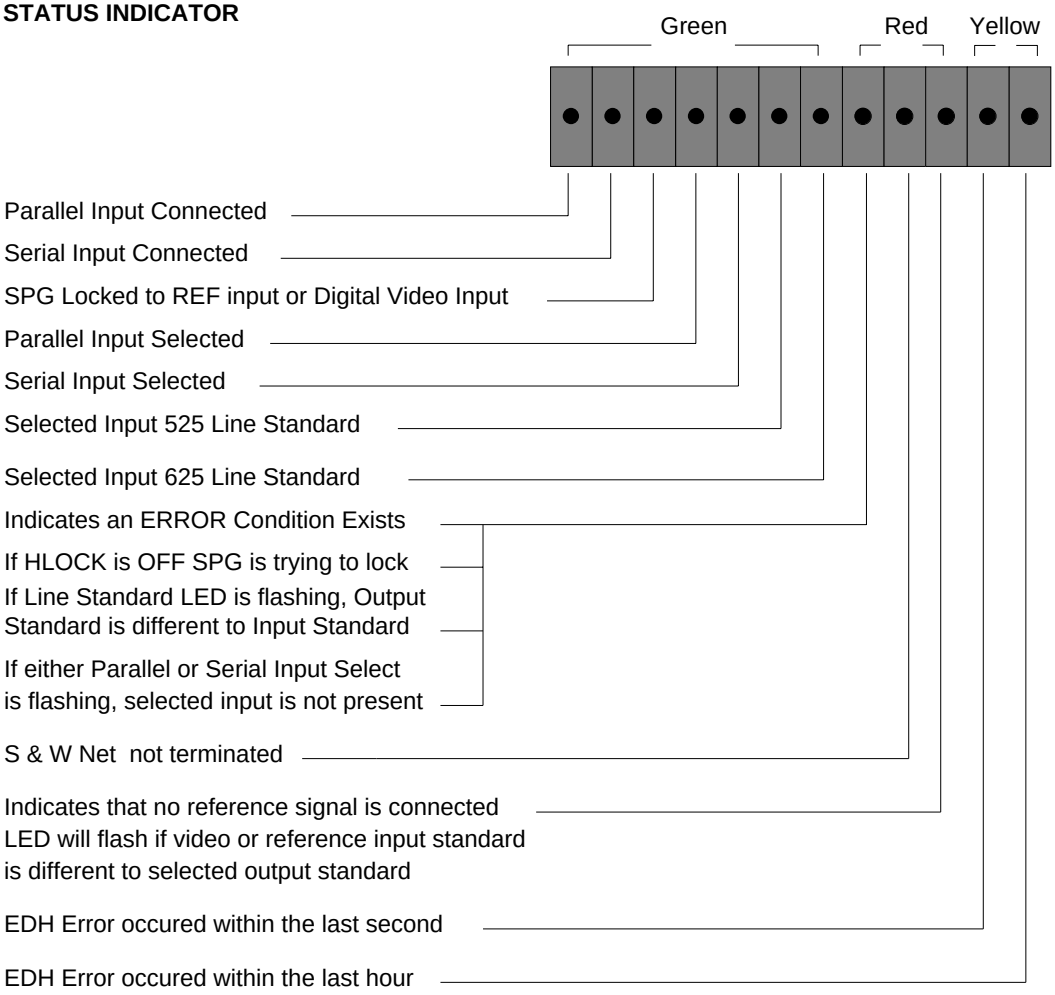
FUNCTION SELECT	SW6 SETTINGS							
	1	2	3	4	5	6	7	8
Input Select Serial	▭							
Input Select Parallel								
Notch Disable		▭						
Notch Enable								
Delay = 1 Line			▭					
Delay = Adaptive up to 1 Frame								
Test Signal Generator OFF				▭				
Test Signal Generator ON								
Sync Amplitude 40 IRE, set-up 7.5 IRE (525)					▭			
Sync Amplitude 300mV, no set-up (525 only)								
Full Bandwidth ‘Q’ signal in 525						▭		
Narrow Bandwidth ‘Q’ signal in 525								
ITS Signal OFF							▭	
ITS Signal ON								
Chroma Bandwidth NORMAL								▭
Chroma Bandwidth WIDE								

Operation

LED STATUS INDICATOR ARRAY

This bank of 12 coloured LED's indicates the status of various functions of the unit.

STATUS INDICATOR

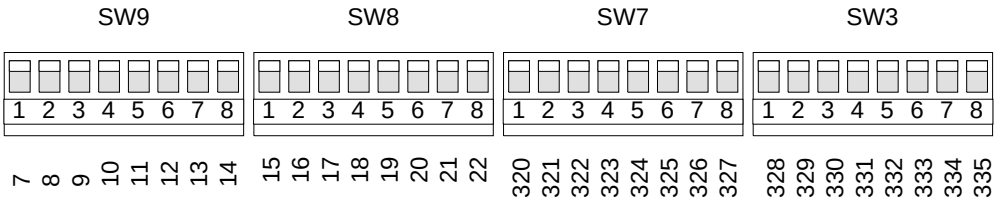


Operation

LINE BLANKING SELECT SWITCHES SW3, SW7, SW8 and SW9

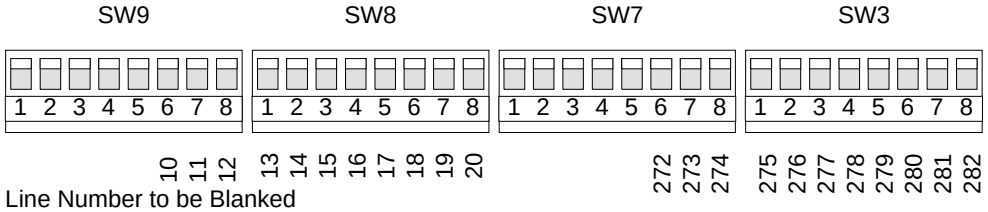
This bank of four 8-way DIL switches allow particular lines of the input signal to be either blanked or passed through the the unit.

625 LINE STANDARD



Line Number to be Blanked

525 LINE STANDARD



Line Number to be Blanked

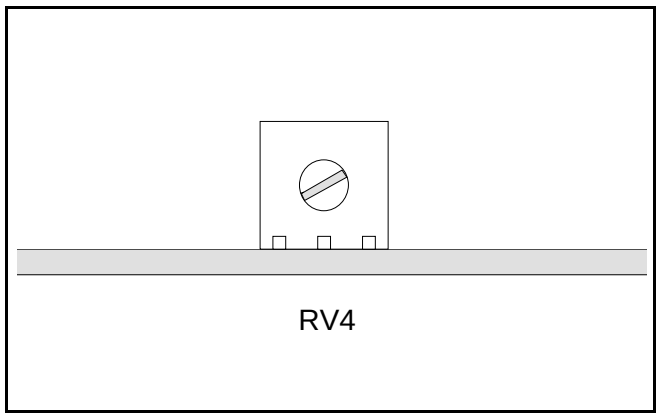
Operation

OUTPUT LEVEL ADJUSTMENT

This control is located on the upper PCB in the mainframe

The overall amplitude of the output signal (Video + Syncs) may be set using this control.

Factory set to give 1V p-p into 75 Ohms.



Operation

1st LINE MAINTENANCE

In the unlikely event of this unit failing to operate correctly no attempt should be made to repair the unit unless all the necessary test equipment, service manuals and technical expertise is available and permission has been granted in writing by SNELL and WILCOX Ltd. or their official agents, for such repairs to be attempted.

Failure to comply with these conditions will void the warranty.

First line maintenance should be confined to the replacement of the plug-in cards, the power supply module, the cooling fan, the air filter and the mains inlet fuse.

CLEANING

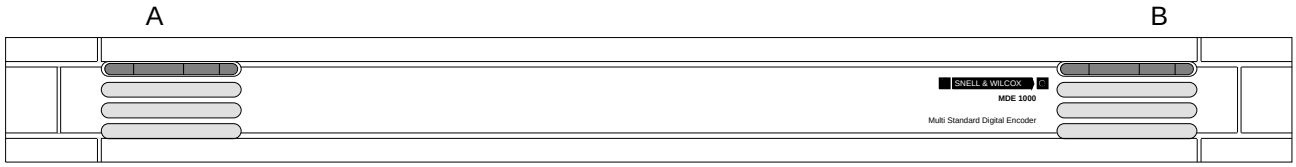
It is important that the ventilation slots in the front and bottom of the front panel and the slots in the side of the unit do not become obstructed or blocked in any way including the build-up of dust etc. as this will interfere with the ventilation and cooling of the unit.

A reduction of air flow through the unit may result in overheating and the power supply over-temperature cut-out may operate and shut down the unit.

The front panel slots, side panel slots and the cooling fan should be regularly inspected and cleaned if necessary.

TO REMOVE THE PCB CARD

The front panel should be pulled forward and down using the two plastic levers A & B to reveal the two circuit cards which may then be safely removed by means of the card ejectors.



IMPORTANT NOTE

The circuit cards must be replaced in their correct locations as shown below. Failure to observe this procedure will render the unit non-operational and may result in damage to the electronics.

Operation

TO REMOVE THE POWER SUPPLY MODULE

1. Disconnect power to the unit by removing the IEC power connector
2. Allow two minutes for capacitors to discharge
3. Remove the top cover of the unit (14 screws)
4. Pull off the white plug-in connectors (2 items)
5. Remove the two M3 countersunk screws on the underside of the case securing the module
6. Withdraw the module

The replacement module is Snell & Wilcox part No. RMY5 UPP100

TO REMOVE THE COOLING FAN

1. Remove the top cover of the unit (14 screws)
2. Remove the two circuit cards using the card ejectors
3. Remove the cable retaining screws from the top of the fan (2 M3 screws)
4. Remove the card-guide-to-frame retaining screws (6 screws) and remove card guide
5. Remove the nut and washer from the stud in front of the fan (M3 nut)
6. Remove countersunk fan retaining screw from underside of case (M3 screw)
7. The fan and its mounting may now be moved into the card space area
8. Remove the fan electrical connections from the front PCB
9. Cut the wires at the connector end to allow removal from the protective sleeving
10. The fan assembly may now be removed from the unit.

The replacement fan is Snell & Wilcox part No. RM F907 (specify either PAPST or Comair type) and has a new connector fitted to the wires which should be retained along the case wall.

Operation

REPLACING/CLEANING THE AIR FILTER

1. The front panel should be pulled forward and down using the two plastic levers
2. Remove the two M3 nuts and washers securing the metal mesh
3. Remove the filter material
4. The filter may be washed in soap and water and replaced when completely dry
5. The filter may be replaced with Snell & Wilcox part No. RMF 806

REPLACING THE MAINS INLET FUSE

The unit has a 3.15AT fuse located in the small pull-out tray of the IEC mains inlet assembly fitted to the rear panel. A spare fuse will also be found in this tray.

The replacement fuse is Snell & Wilcox part No. RMF 3.15AT

END.

Appendix 1

PROPOSED SMPTE STANDARD FOR FAULT REPORTING IN TELEVISION SYSTEMS

SMPTE269M

1 SCOPE

This standard describes a simple interface over which television equipment can report the occurrence of internal failures and faults in incoming signals. It is intended for use in all television equipment, from the simplest active device to the most complex.

The interface consists of an isolated closure which can assume one of three states: open, closed or pulsing. These respectively signal that the reporting device is okay, has detected an internal fault, or is detecting incoming signal faults.

Fault occurrence data may be collected from equipment complying with this standard by several means, ranging from simple "follow the lights to the trouble" summary alarm schemes to computerised logging systems.
While full specification of such systems is beyond the scope of this standard, a general outline of one possible implementation is given in annex A.

2 NORMATIVE REFERENCE

The following standard contains provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below.

IEC 169-8 (1978), R.F. Coaxial Connectors with Inner Diameter of Outer Conductor 6.5 mm (0.256 in) with Bayonet Lock - Characteristic Impedance 50 Ohms (Type BNC)

3 FAULT STATES

3.1 A reporting device may be one of three states:

3.1.1 Normal operation

The device is currently not detecting any internal failures and is receiving power.

3.1.2 Internal failure

The device is currently detecting an internal failure or has lost power.

3.1.3 Incoming signal fault

The device is not detecting any internal failures, but is currently detecting fault in incoming signal(s).

Appendix 1

4 INTERFACE DEFINITION

4.1 Interface

The interface consists of two-wire connection from an electrically-isolated output closure in the reporting device. The interface reports faults only at the times that they are detected. The closure may be in one of three states:

4.1.1 Open

An open output signifies that the reporting device is operating correctly with valid input(s).

4.1.2 Closed

A closed output signifies that the reporting device has detected an internal fault or has lost power. The closure last s only for the duration of the fault.

4.1.3 Pulsing

A pulsing output signifies that the reporting device has detected errors in the signal(s) it is receiving. The pulsing lasts only for the duration of the errored field(s).

4.2 Pulsing

Pulsing is defined as a closed pulse from 1-2 ms long occurring once per field.

5 ELECTRICAL CHARACTERISTICS

5.1 Output

The output of the reporting device is a closure, electrically isolated from the rest of the device. The isolating mechanism shall withstand a common-mode potential of 60 V peak at frequencies from DC to 400 Hz. The shell of the connector may be bypassed to the chassis by a small-value capacitor, if needed, to limit rf radiation.

5.2 Output closure

The output closure must be in the closed state when power is removed from the device (see annex A).

5.3 Open state characteristics

When in the open state, the leakage across the closure must be less than 100 uA at any voltage from 0V to 5 V DC. The closure shall be able to withstand 24 V DC in the open state without damage.

5.4 Closed-state characteristics

In the closed state, the maximum voltage drop across the closure shall not exceed 2V at 20mA. The sensing device shall not supply more than 20mA of current to the reporting device.

Appendix 1

6 CONNECTOR

The chassis connector used shall be a female BNC type, as defined in IEC 169-8. The center contact shall be connected to the positive side of the sensing mechanism.

Note - Only the mechanical dimensions are specified. Both 50- and 75-ohm connectors are available which meet these requirements.

ANNEX A (informative)

Possible implementation of a reporting scheme

There are many ways to implement a fault data collection and reporting system using the interface specified in this standard. The implementation described here is one of the simplest. It is a hierarchical system and is designed to lead a technician to the faulty device by means of visual and audible signals. No provision is made for automated logging of faults; however, such logging is not precluded.

The scheme works as follows:
All fault reporting outputs in each rack or frame are connected in parallel to a summary alarm repeater, which consists of a power supply, an optoisolator circuit, and an alarm lamp and driver, as shown in figure A 1.

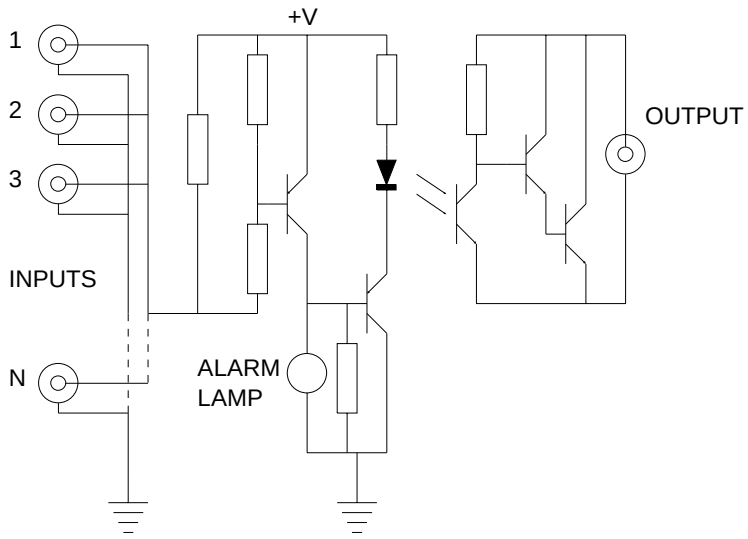


Figure A.1.-Reporting Scheme Implementation

The outputs of the repeaters are connected in parallel to an identical repeater at the end of the rack row. These in turn are connected to another repeater at the entrance to the rack area, and so forth, until all alarms are summed at a staffed monitoring point. Audible alarms may also be used where desired.

When an alarm occurs, the technician simply follows the lights to the correct room, rack area, rack row, rack, frame, and faulty module, and either resets or replaces it as required.
Note that this scheme relies on the device originally reporting the fault to provide visual indication of the fault condition.
Schemes of this type have been used by telephone companies for years. They are simple to design and inexpensive to implement. Although they do not provide detailed fault logging, as noted, they greatly facilitate locating failures.

Appendix 1

ANNEX B (informative)

Output loss detection

The requirement to signal loss of power as a fault implies that the output must revert to the closed state when the power is off. Figure B.1 shows one possible implementation of such a circuit.

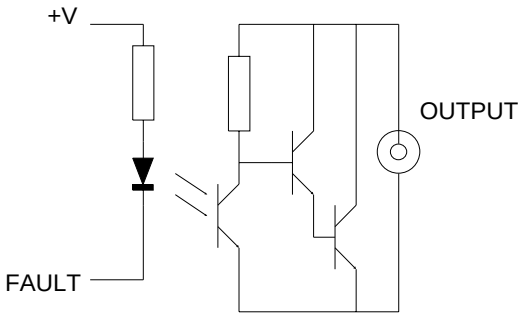


Figure B.1.-Output Interface Implementation

ANNEX C (informative)

Output loss detection

Normal analog video system design practice is to have all outputs of a device driven by the same active components, with the different outputs isolated from each other by buildout resistors. With this arrangement, one can determine the condition of all outputs of the device with a high degree of confidence by monitoring only one of them.

In digital television systems, the bandwidths involved make commonly-driven resistively-isolated outputs impractical. Instead, each output is typically driven by a separate active stage, and noise considerations frequently dictate that half the output drivers are fed from the Q output of the previous stage, while the other half are fed by the not-Q output.

Given this topology, monitoring one output of a device does not indicate the health of the other outputs to the degree of confidence required. The only way to provide this level of confidence is for the device itself to monitor all outputs internally, signaling a fault if any of them fails while the device is receiving or generating a valid input.

ANNEX D (informative)

Bibliography

SMPTE 259M, Television--10-bit 4:2:2 Component and 4 fsc NTSC Composite Digital Signals -- Serial Digital Interface SMPTE RP165, Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television.

Appendix 2

PROPOSED SMPTE RECOMMENDED PRACTICE RP165

Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television

1 SCOPE

1.1

This practice describes the generation of error detection checkwords and related status flags to be used optionally in conjunction with the serial digital interface for system M (525/59.94) and systems B, G, H and I (625/50) digital television equipment operating with either 4:2:2 component digital signals of $4f_{SC}$ composite digital signals. Although it is preferred that this error checking method be used in all serial transmitters and receivers, it is recognised that some equipment must minimise complexity.

NOTE - Line numbers in tables 2 and 3 for 625/50 systems are tentative, and subject to change pending decisions on vertical interval switching for serial signals.

1.2

Two checkwords are defined: one based on a field of active picture samples and the other on a full field of samples. This two-word approach provides continuing error detection for the active picture when the digital signal has passed through processing equipment that has changed data outside the active picture area without re-calculating the full-field checkword.

1.3

Three sets of flags are provided to feed forward information regarding detected errors to help facilitate identification of faulty equipment. One set of flags is associated with each of the two field related checkwords. A third set of flags is used to provide similar information based on evaluating all of the ancillary data checksums within a field.

1.4

The checkwords and flags are combined in an error data packet which is included as ancillary data i the serial digital signal. At the receiver, a recalculation of checkwords may be compared to the error data packet information to determine if a transmission error occurred.

Appendix 2

2 NORMATIVE REFERENCES

The following standards contain provisions which, through reference in this text, constitute provisions of this practice. At the time of publication, the editions indicated were valid. All standards re subject to revision, and parties to agreements based on this practice are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below:

ANSI/SMPTE 125M-1992, Television - Component Video Signal 4:2:2 - Bit-Parallel Digital Interface

SMPTE 244M, Television - System M/NTSC Composite Video Signals - Bit-Parallel Digital Interface

SMPTE 259m, Television - 10-Bit 4:2:2 Component and 4_{fsc} NTSC Composite Digital Signals - Serial Digital Interface

SMPTE RP 168, Definition Of Vertical Interval Switching Point for Synchronous Video Switching

ICE 60B(Sec)200, Helical-Scan Digital Composite Video Cassette Recording Using 19mm Magnetic Tape (Format D-2) (NTSC, PAL), Section Five, Video Interface

EBU Tech 3267- E, Parallel Interface for 625-Line Digital Video Signals

Appendix 2

3 LOCATION OF CHECKWORDS, FLAGS, AND INCLUDED SAMPLES

3.1 Location of Checkwords and Flags

Digital data packets containing the calculated checkwords and error information flags are located in the ancillary data area of the vertical interval in a manner to complement the recommended practice of source switching. Locations are shown graphically in figure 1 and specified in table 1 for 525/59.94 systems and table 2 for 625/50 systems. For composite signals, the error data packet is located in the ancillary data area of the first horizontal pulse occurring in the line prior to the recommended vertical interval switching point of each field. For component signals, the error data packet is located just prior to SAV (start of video) in the same lines. To enable proper operation of equipment implementing this practice, signal switching must take place in the vertical interval and conform to SMPTE RP 168.

	Vertical Blanking Interval
ccc fff	(Line n with last full-field sample) eef (Line n+1 with error data packet) (Line n+2 used for switching) (Line n+3 not included in full-field sample) (Line n+4 first full-field sample)
	aaa (Line with first active picture sample)
H-interval Samples not contained in active picture checkword	Active Picture Area (see 3.2 for definition)
	(Line with last active picture sample) eea

NOTES
1 See Tables 1 and 2 for exact sample locations in both fields.
2 ccc = location of checkwords and status flags
3 fff = first sample included in the full-field checkword
4 aaa = first sample included in the full-field checkword
5 eea = last sample included in the active picture checkword.
6 eef = last sample included in the full-field checkword

Figure 1-Location of Checkwords and Included Samples

Appendix 2

Table 1-Location of 525/59.94 System Checkwords

Data Item	Composite	Component
Error checking data locations		
Line 9 fields 1 & 111, Line 272,fields 11 &1V		
Ancillary data header, word 1 - component		1689 (000_h)
Ancillary data header, word 2 - component		1690 ($3FF_h$)
Ancillary data header, word 3 - component		1691 ($3FF_h$
Auxiliary data flag - composite	795 ($3FC_h$)	
Data ID	796 ($1F4_h$)	1692 ($1F4_h$)
Block number	797 (200_h)	1693 (200_h)
Data Count	798 (110_h)	1694 (110_h)
Active picture data word 0	799	1695
Active picture data word 1	800	1696
Active picture data word 2	801	1697
Full-field data word 0	802	1698
Full-field data word 1	803	1699
Full-field data word 2	804	1700
Ancillary data error flags	805	1701
Active picture error flags	806	1702
Full-field error flags	807	1703
Reserved words (7 total)	808-814 (200_h)	1704-1710(200_h)
Checksum for this ancillary data block	815	1711

Appendix 2

Table 2 - Location of 625/50 System Checkwords

Data item	Composite	Component
Error checking data locations:		
Line (5) fields 1 & 111, Line (318), fields 11&1V		
Ancillary data header, word 1 - component		
Ancillary data header, word 2 - component		$C_r425(3FF_h)$
Ancillary data header, word 3 - component		Y851 ($3FF_h$)
Auxiliary data flag - composite	972 ($3FC_h$)	
Data ID	973 ($1F4_h$)	C_b 426 ($1F4_h$)
Block number	974 (200_h)	Y852 (200_h)
Data count	975 (110_h)	C_r426 (110_h)
Active picture data word 0	976	Y853
Active picture data word 1	977	C_b427
Active picture data word 2	978	Y854
Full field data word 0	979	C_r427
Full field data word 1	980	Y855
Full field data word 2	981	C_b428
Ancillary data error flags	982	Y856
Active picture error flag	983	C_r428
Full field error flags	984	Y857
Reserved words (7 total)	985-991 (200_h)	C_b429-C_r430 (200_h)
Checksum for this ancillary data block	992	Y861

NOTES

1 Values in the tables are word numbers for the appropriate standard.
2 Values in parentheses are sample values.
3 625/50 line numbers (in brackets) are tentative.

Appendix 2

3.2 Samples included in checkword calculations

Starting and ending samples for active picture and full-field checkword calculations are shown in table 3. For the active picture checkword, only the samples in the active picture area of each line are included in the calculation. As used in this practice, the active picture includes only those lines which, in composite systems, are full lines (that is, half lines are not included.) Full-field checkwords include all the samples in all lines except the line containing the error data packet and the two following lines. The line following the error data packet is normally used for vertical interval switching and the next line is excluded to ensure that word framing and TRS propagation are restored after a switch.

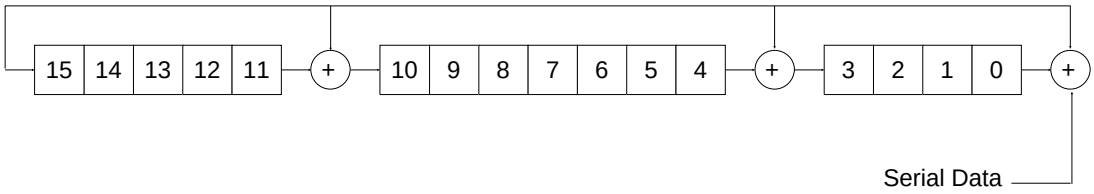
NOTE - For the purpose of performing the CRC calculations in PAL composite systems, sample 967 is defined as the TRS sample with value $3FF_h$. This is consistent with IEC 60b (Sec)200, but must be clearly defined for CRC calculations in a case a nonstandard horizontal interval is encountered.

4 DEFINITION OF DATA WORDS

4.1 Checkword values

Each checkword value consists of 16 bits of data calculated using the CRC-CCITT polynomial generation method. The equation and a conceptual logic diagram are shown below:

Checkword (16 Bit) = $X^{16} + X^{12} + X^5 + 1$



4.2 Ancillary Date Housekeeping, Checkwords, and Flags

Definitions of each ancillary data word specified by this practice are shown in table 4. To provide compatibility with 8-bit equipment, 0s are used in the two least significant bits of all words in the data packet. Bit b7 (V) in picture/field data word 3 is a 1 if a valid CRC has been calculated. This allows implementations which calculate only one or the other of the checkwords. A P in b8 provides even parity for b7 through b0; that is, the total number of 1s in b8 through b0 is an even number. The most significant bit, b9, is the logical inverse of b8. A checksum is the last word in the error data packet as required by the ancillary data formatting for the serial digital interface.

The checksum word is used to determine the validity of the included words. The checksum word shall consist of 9 bits and the sum of the 9 least significant bits (b8 through b0) of all words including Data ID through reserved words. Preset to all zero at the start of each calculation and ignore the carry.

Appendix 2

4.3 Error Flags

All error flags indicate only the status of the previous field; that is, each flag is set or cleared on a field-by-field basis. A logical 1 is the set state and a logical 0 is the unset state. The flags are defined as follows:

edh - error detected here:
Signifies that a serial transmission data error was been detected. In the case of ancillary data, this means that one or more ANC data blocks did not match its checksum.

eda - error detected already:
Signifies that a serial transmission data error has been detected somewhere upstream. If device B receives a signal from device A and Device A has set the edh flag, when B re transmits the data to device C, the eda flag will be set and the edg flag will be unset if there is no further error in the data.

idh - internal error detected here:
Signifies that a hardware error unrelated to serial transmission has been detected within a device. This is provided specifically for devices which have internal data error checking facilities, as an error reporting mechanism.

ida - internal error detected already:
Signifies that an idh flag was received and there was a hardware device failure somewhere upstream.

ues - unknown error status:
Signifies that a serial signal was received from equipment not supporting this error-detection mechanism.

Table 3-Checkwords Included Samples

Data Item	Composite	Component
525.59.94 systems		
First full-field sample, lines 12 and 75	795	1444
First active picture sample, lines 21 and 284	0	0
Last active picture sample, lines 262 and 265	767	1439
Last full-field sample, lines 8 and 271	767	1439
625/50 systems		
First full-field sample, lines (8) and (421)	972	C_b361
First active picture sample, lines 24 and 336	0	C_b0
Last active picture sample, lines 310 and 622	947	Y719
Last full field sample, lines (4) and (317)	947	Y719

NOTE - Full-field 625/50 line numbers (in brackets) are tentative

Appendix 2

Table 4-Definition of Ancillary Data Words

Data item	b9 msb	b8	b7	b6	b5	b4	b3	b2	b1	b0 lsb
Ancillary data header, word 1 - component	0	0	0	0	0	0	0	0	0	0
Ancillary data header, word 2 - component	1	1	1	1	1	1	1	1	1	1
Ancillary data header, word 3 - component	1	1	1	1	1	1	1	1	1	1
Auxiliary data flag - composite	1	1	1	1	1	1	1	1	0	0
Data ID	0	1	1	1	1	1	0	1	0	0
Block number	1	0	0	0	0	0	0	0	0	0
Data count	0	1	0	0	0	1	0	0	0	0
Active picture data word 0 crc:<5:0>	$\overline{P}$	P	c_5	c_4	c_3	c_2	c_1	c_0	0	0
Active picture data word 1crc:<1 1:6>	$\overline{P}$	P	c_{11}	c_{10}	c_9	c_8	c_7	c_6	0	0
Active picture data word 2 crc<15:12>	P	P	V	0	c_{15}	c_{14}	c_{13}	c_{12}	0	0
Full field data word 0 crc<5:0>	$\overline{P}$	P	c_5	c_4	c_3	c_2	c_1	c_0	0	0
Full field data word 1 crc<11:6>	$\overline{P}$	P	c_{11}	c_{10}	c_9	c_8	c_7	c_6	0	0
Full field data word 2 crc<15:12>	P	P	V	0	c_{15}	c_{14}	c_{13}	c_{12}	0	0
Auxiliary data error flags	$\overline{P}$	P	0	ues	ida	idh	eda	edh	0	0
Active picture error flags	$\overline{P}$	P	0	ues	ida	idh	eda	edh	0	0
Full field error flags	$\overline{P}$	P	0	ues	ida	idh	eda	edh	0	0
Reserved words (7 total)	$\overline{1}$	0	0	0	0	0	0	0	0	0
Checksum	$\overline{S8}$	S8	S7	S6	S5	S4	S3	S2	S1	S0

NOTE - P and V are defined in 4.2

End.