VISTEK V1621
ANALOGUE TO DIGITAL
CONVERTER USER GUIDE

www.pro-bel.com

Contents

1. OVERVIEW

The V1621 Precision 10 Bit ADC Module provides 10 - bit precision conversion between RGB or YPbPr component input signals and provides four Serial Digital Outputs.

Flexible user configuration via programming switches assures elegant implementation in most systems. SMPTE/EBU N10 component levels or Betacam levels can be configured independently for 525/60 and 625/50 modes of operation. The module itself will automatically detect the incoming reference standard and convert appropriately using the defined levels in each standard.

Comprehensive options for set up in 525 line mode are also provided.

Remote interface is available for remote control.

Full Specification CCIR 601 filters are used to ensure full compatibility and system integrity. A lower cost option is available using near 601 performance filters.

2. IMPORTANT FEATURES

- Full 10 Bit Precision
- User selectable configuration
- Full specification CCIR 601 filtering
- 4 x Serial outputs
- RGB or YPbPr Inputs

3. INTRODUCTION

This section gives information on installing the V1621 ADC modules into the V1603 interface frame and details on the connections that can be made to it. Information is also supplied on the function of each preset adjustment and switch which is made available to the user on the front panel, and the module PCB.

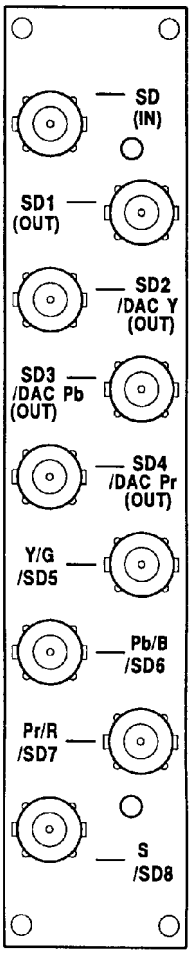
4. INSTALLING MODULES

The V1603 and V1601 frames are normally supplied with modules fitted. However, if further modules are to be fitted to a part loaded unit follow the instructions below.

Remove the screws from the blanking plate covering the spare position at the rear of the equipment and remove the plate. Place the new rear module into the frame and slide in until the connector(s) mates. The connector panel on the rear module should be seated flush with the rear cross extrusions of the frame when inserted correctly. Secure the module to the rear cross extrusions with the screws provided.

5. REAR PANEL CONNECTIONS

All the input and output connections are available on the rear panel as shown below.



5.1 Y/G, Pb/B, Pr/R Inputs

These BNC connectors are internally terminated with 75 Ohms. The analogue components should be connected to these.

5.2 Ref Input (S/ SD8)

If the unit is to be locked to an external reference (as opposed to syncs on Y /G), the external reference may be connected here. External Reference or Syncs on Y /G may be selected by the External Syncs switch SW12 on the ADC module.

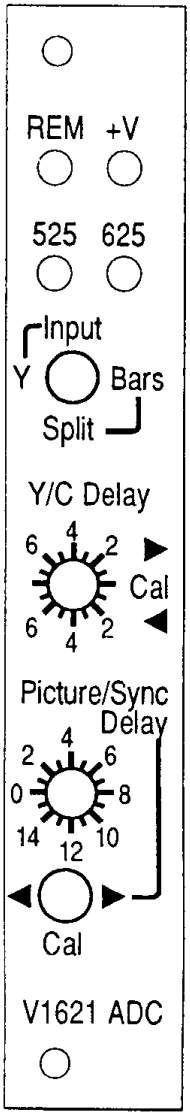
The nominal external reference level may be either High Level (2 to 4 Volts mixed syncs) or Low Level (1 Volt composite reference with 300 mV syncs with or without colour burst). The nominal external reference level should be selected by the Low Syncs switch SW13 (see below) on the ADC module. The unit will continue to lock even if the references are 6 dB below nominal level.

5.3 Serial Digital Outputs: SDI (OUT) - SD4 (OUT)

These are four identical serial digital outputs to SMPTE T14.22/082.

6. FRONT PANEL INDICATORS

A view of the front panel controls and switches is shown below.



+V lamp

Indicates that power is applied to the module.

REM lamp

Indicates that the module/control system communications link is active.

525 lamp

Indicates that the unit is working in 525 mode and that it is locked to the input reference (either syncs on Y/G or External Reference). If the input reference disappears the lamp will go out.

625 lamp

Indicates that the unit is working in 625 mode and that it is locked to the input reference (either syncs on Y/G or External Reference). If the input reference disappears the lamp will go out.

7. FRONT PANEL CONTROLS

7.1 Y, Input, Bars & Split

This is a 4 position rotary switch that functions as follows:
The arrow pointer indicates the type of signal selected.

Input

When pointing vertically upwards the Input is selected.

Bars

When pointing to BARS a 100% Colour Bars test signal is selected.

Split

When pointing to SPLIT a Ramp (1/4 picture height) plus 100% Colour Bars (1/4 picture height) plus the input signal (1/2 picture height) is selected. The test pattern is the same in 525 and 625 modes.

Y

When pointing to Y (Monochrome) the chrominance input channels are disabled and the module outputs grey level instead for the colour difference signals.

7.2 Y/C Delay Rotary Switch

This switch is intended to correct for horizontal timing errors in the input picture luminance relative to the input picture chrominance. The switch moves the Luminance component of the picture horizontally by 16 steps of 74 ns. The calibrated position for the switch is Cal.

7.3 Picture/Sync Delay Toggle Switch and Rotary Switch

These switches are intended to correct for horizontal timing errors in the input picture relative to the input reference.

These switches together move the picture horizontally relative to the line reference signal.

The rotary switch moves the picture position horizontally by 16steps of 74 ns.

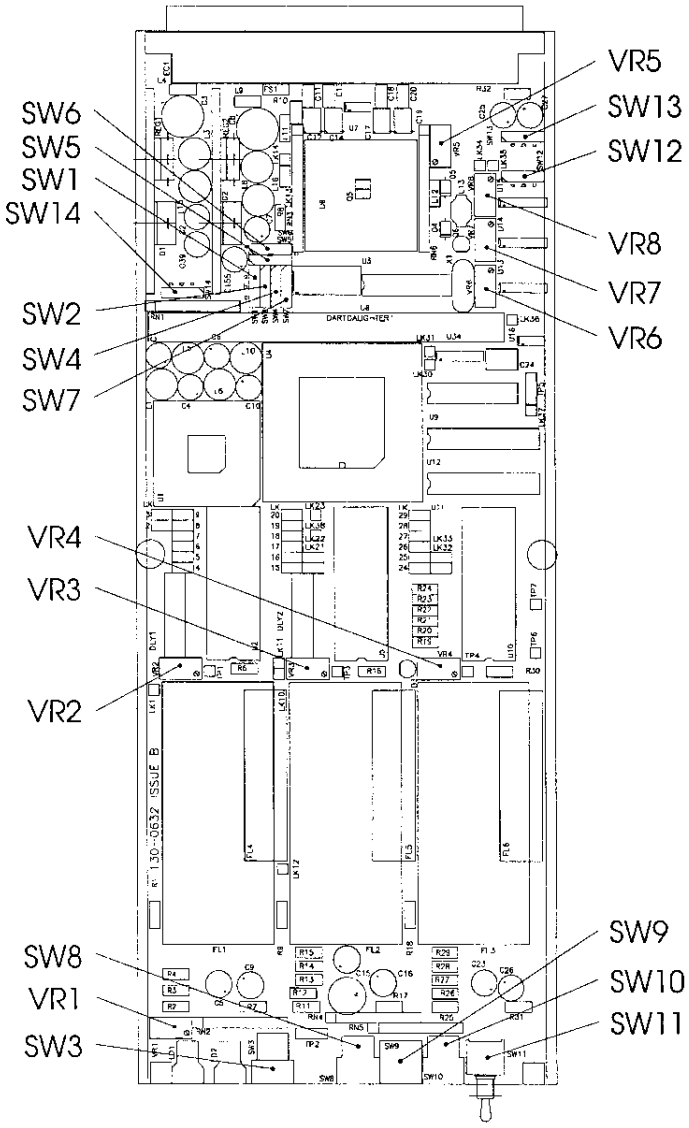
The Advance/Delay (+/-) switch selects the direction of the horizontal picture shift.

The calibrated positions for these switches is 0 for the rotary switch and Cal for the Picture Advance/Delay toggle switch.

8. ON BOARD CONTROLS AND ADJUSTMENTS

Locations of switches and preset potentiometers are shown below.

To gain access to these controls and adjustments the board must be removed from the chassis. If the adjustments need to be made while the unit is powered up, an extender card needs to be used.



When reference is given to the direction/position of switch settings, it assumes that the module is in the vertical position as in the rack with the control panel on the left.

8.1 Y, Pb, Pr Gain Preset Potentiometers

VR2, VR3 and VR4 adjust the gain of the y, Pb and Pr channels respectively.

8.2 Setup Preset Potentiometer

VRl may be adjusted to remove the setup (if any) on a 525 standard input The calibrated level is for a 7.5 I.R.E. pedestal and the range of this control is from 0 to approximately 15 I.R.E. Be aware that this control is inoperative if the Setup switch is set in the DOWN position.

The gain and setup potentiometers are calibrated in the factory before delivery, the unit will need to be re-calibrated if the settings are altered (see calibration section).

8.3 Setup Switch

When SW6 is set in the DOWN position, the pedestal on a 525 input will be removed. When set in the UP position the pedestal will not be removed. Due to internal processing, the precise width of the pedestal is unimportant.
The Setup Preset Potentiometer can be adjusted for non-standard pedestal amplitudes.
The Setup function is inoperative when the unit is in 625 mode.

8.4 Auto Switch and 525-625 Switch

When SW14 is set in the UP position, the unit will automatically detect the standard on the input reference and adjust itself to this standard.
When SW14 is set in the DOWN position, the unit is forced to the standard selected by SW5.
When SW5 is set in the UP position 525 line mode is selected.

When SW5 is set in the DOWN position 625 line mode is selected.

If SW14 is set in the UP position, and the reference disappears, the 11nit will free-run in the last standard to which it was locked.

8.5 BETA 625 and BETA 525 Select Switches

The gain levels given below assume that the gain of the unit is correctly calibrated, that is the Y Pb, and Pr gain potentiometers are correctly set.

When SW2 is set to the RIGHT and the unit is in 625 mode, the gain levels for the Y, Pb, Pr channels are set for 625 N10 levels (700 mV black to peak white on Y, 700 mV peak to peak on Pb and Pr for 100% Colour Bar signal). When SW2 is set to the LEFT and the unit is in 625 mode, the gain levels for the Y, Pb, Pr channels are set for 625 Beta levels (700 mV black to peak white on Y, 933 mV peak to peak on Pb and Pr for 100% Colour Bar signal).

When SW4 is set to the RIGHT and the unit is in 525 mode, the gain levels for the Y, Pb, Pr channels are set for 525 N10 levels (700 mV black to peak white on Y, 700 mV peak to peak on Pb and Pr for 100% Colour Bar signal).

When SW4 is set to the LEFT and the unit is in 525 mode, the gain levels for the Y, Pb, Pr channels are set for 525 Beta levels (660 mV black to peak white on Y, 933 mV peak to peak on Pb and Pr for 100% Colour Bar signal).

8.6 RGB Slide Switch

If the analogue component inputs are to be Colour Difference signals (y, Pb, Pr) then SW7should be set to the RIGHT and the internal RGB to Y, Pb, Pr matrix will be bypassed.

If the analogue component inputs are to be G, B, R signals then SW7 should be set to the LEFT and the internal RGB to Y, Pb, Pr matrix will be enabled.

8.7 Cal Y Timing Rotary Switch

This switch is adjusted to ensure that the setting for the front panel Y timing rotary switch is CAL when the luma/ chroma timing is correct. Instructions for adjustment are given in the Calibration section.

External Syncs slide switch

When SW12 is set in the UP position the unit is locked to syncs on Y / G.
When SW12 is set in the DOWN position the unit is locked to the external reference.

8.8 Low Syncs Slide Switch

When SW13 is set in the UP position the unit is configured for a low level external reference.
When SW13 is set in the DOWN position the unit is configured for a high level external reference.

This switch has no effect if the internal reference is being used.

(For level information, see Ref. Input section under Rear Module Connections earlier in this document)

8.9 Vertical Blanking Switch

When SW1 is set to the RIGHT any video appearing on the active line during vertical blanking is blanked out. These are lines 1 to 9 and 264 to 272 in 525 mode, and lines 624 to 22 and 311 to 335 in 625 mode.
If SW1 is set to the LEFT, video appearing on any lines in the vertical blanking period is not removed.

8.10 Y, U and V Delay Headers and Links

These allow fine timing adjustment of the Y, Pb and Pr horizontal timing in 5 ns steps. Instructions for adjustment are given in the Calibration section.

8.11 Free Run Frequency Preset Potentiometer

VR6 sets the oscillator frequency when the unit is not being locked to a reference. Instructions for adjustment are given in the calibration section.

8.12 Mark/Space Preset Potentiometer

VR8 adjusts the 27 MHz clock mark / space ratio to 50/50. Instructions for adjustment are given in the calibration section.

8.13 Fine H Timing/Phase Preset Potentiometer

VR7 adjusts the horizontal picture position relative to the TRS (Timing Reference Signal) pulses. Instructions for adjustment is given in the calibration section.

8.14 Serialiser Free Run Frequency Preset Potentiometer

VR5 sets the serialiser oscillator centre frequency. Instructions for adjustment are given in the calibration section.

Table 1: Switch location and their functions

Switch Location	Setting	Function
SW1	Right Left	Vertical blanking on Vertical blanking off
SW2	Right Left	625 N10 levels 625 Beta levels
SW4	Right Left	525 N10 levels 525 Beta levels
SW5	Up Down	525 Mode 625 Mode
SW6	Up Down	Pedestal On Pedestal removed
SW7	Right Left	YpbPr RGB
SW12	Up Down	Locked to Y/G sync Locked to external reference
SW13	Up Down	Low level reference syncs High level reference syncs
SW914	Up Down	Auto standard detection Manual standard detection

Table 2: Preset controls and their functions

Preset Control	Function
VR1	Insert pedestal, 0-15 IRE
VR2	Y gain adjustment
VR3	Pb gain adjustment
VR4	Pr gain adjustment
VR5	Set serialiser oscillator centre frequency
VR6	Set free running 27 MHz oscillator
VR7	Horizontal picture position relative to the TRS adjustment
VR8	27MHz oscillator mark / space ratio

Table 3: Links and their functions

Link number	Function
LK2 to LK9	Y/C delay on Y channel
LK1, LK10, LK11	Test points for Y,U,V clamp
LK12	Test point for 525 set up level
LK13, LK14	Link/Test point for free running 27 MHz alignment
LK15 to LK22	Y/C delay for Cb channel
LK23	Test point for checking 27MHz clock
LK24 to LK29 and LK32, LK33	Y/C delay for Cr channel
LK30	Test point for 47 us pulse reference for clock generation
LK31, LK36	Test points for 27 MHz PLL clock generation
LK34	Test point for signal present indication
LK35	Test point for checking internal/external sync
LK37	Test point for checking mixed syncs
LK38	Test point for H timing adjustment, using clamp pulse and line sync

9. CALIBRATION OF V1621 ADC MODULE

9.1 Introduction

This section is intended to provide sufficient information to allow an engineer to calibrate the ADC system. Calibration should only be carried out if the unit has been mal-adjusted, or if drift has occurred over an extended period of time.

It should be appreciated that calibration is not a duplication of the alignment procedure, which should be referred to if a repair has been carried out to the module.

9.2 Test Equipment

100 MHz dual channel oscilloscope.
Tektronix TSG300 dual standard Component Test Signal Generator or equivalent.

525 Test Signal Generator capable of providing 7.5 I.R.E. pedestal on Y.

Dual standard television waveform monitor.

Frequency Counter capable of measuring 27 MHz TTL signal with accuracy better than 5 ppm.

Vistek V1222/V1624 dual standard serial digital to Analogue Component Video converter or equivalent.

Two 75 Ohm adjustable delay lines, 20 ns total adjustable in 1 ns steps.

Test signal generator with bowtie component serial digital output for pre-calibration of test equipment setup.

9.3 Environmental

The calibration should be carried out at a nominal temperature of 20 degrees Celsius.

9.4 Test Equipment Connection

Connect the Y, Pb, Pr outputs of the TSG300 or similar test pattern generator to the Y, Pb, Pr inputs of the unit under test. Use cables of the same type and equal length (this is necessary for luma-chroma delay calibration).

Connect one of the serial digital outputs from the unit under test to the Vistek V1624 10 bit serial digital to Analogue Component Video converter. Connect the outputs of the V1624 to the television waveform monitor. The V1624 Luma/Chroma delay including delays through cables should be calibrated at the waveform monitor using a digitally generated bowtie test pattern input to within plus or minus 1 ns, if necessary using the adjustable delay lines in the cables.

9.5 Calibration Procedure

Initial Setup: Set

A SW12 UP / Internal sync on Y
B SW13 UP / Low sync. level
C SW7 Right / YPbPr Input
D SW14 and SW5 Down / Force 625 operation
E SW3 position 0 / Input source to output
F SW9 position 4 / Engineering Y/C delay
G SW10 position 0 / Zero picture / sync delay
H SW8 Position CAL / front panel Y/C delay
I SW11 Centre position

9.6 Clock Centre Frequency and Mark / Space Calibration

Remove signal from Y Input to unit under test and check that 625 Locked and 525 Locked front panel LEDs are off.

Using a frequency counter, monitor LK23 and adjust VR6 for 27 MHz +/-1 Hz.

Apply a signal to the Y input; verify that the frequency on LK23 remains constant.

Using an oscilloscope monitor LK23 and adjust CR8 for 50:50 mark space ratio.

Verify that the 625 LED is illuminated.

9.7 Luma / Chroma Timing

Select 625 lines 100% Y, Pb, Pr Colour bars on test pattern generator (with syncs on Y).

Ensure that front panel Y Timing rotary hex switch is set to CAL. Set coarse Luma/Chroma timing using the on board Cal Y Timing rotary hex switch so that luminance and chrominance colour bar transitions are approximately co-timed.

Select 625 lines Bowtie on test pattern generator (with syncs on Y).

Set fine Luma/Chroma timing using Y Delay, U Delay and V Delay programmable links so that Y, Pb, and Pr are co-timed to within 5 ns. Only one of the 8 available link positions in each channel should be fitted. A further adjustment of the Cal Y Timing rotary hex switch may be necessary, as the total link adjustment range on each channel is 35 ns (in 5 ns steps).

9.8 Gain Adjustment

Select 625 lines 100% Y, Pb, Pr Colour bars on test pattern generator (with syncs on Y). Set the front panel Bars switch to down for Split.

Adjust VR2 gain preset potentiometer so that the amplitude of the Y input signal, and the Y signal on the digitally generated bars are equal when measured on the Waveform Monitor.

Adjust VR3 gain preset potentiometer so that the amplitude of the Pb input signal, and the Pb signal on the digitally generated bars are equal when measured on the Waveform Monitor.

Adjust VR4 gain preset potentiometer so that the amplitude of the Pr input signal, and the Pr signal on the digitally generated bars are equal when measured on the Waveform Monitor.

9.9 Setup adjustment

Select any 525 lines signal with 7.5 I.R.E. pedestal on test pattern generator. Ensure that Setup switch SW6 is in the up position. Adjust VR1 potentiometer so that pedestal is removed when viewed on waveform monitor.

H Timing adjustment

This adjustment requires that the Colour bar, green/magenta transition on the Test Pattern Generator, driving the inputs to the board occurs in the centre of the 720 pixels of the active line. Select 625 lines 100% Y, Pb, Pr colour bars on the test pattern generator (with syncs on Y). Set the front panel Bars. Set the front panel BAR to SPLIT.

Adjust the fine H timing Preset VR7 so that the transitions between the green and magenta bars on the top half of the picture (digitally generated) and the bottom half of the picture (from the input) are co-timed to within 10 ns.

Alternatively, using scope and scope probes, simultaneously monitor LK38 and R1. Adjust VR7 so that the analogue clamp pulse starts 2.2 us after line sync.

9.10 Serialiser Free Run Oscillator Setup

Fit LK13. Using frequency counter, monitor LK14. Adjust VR5 for 27.000 MHz +/- 1Hz. Remove LK13. Verify frequency remains locked at 27.000 MHz.

This completes the V1621 ADC Module Front Panel Board calibration.