



VISTEK V1624 DIGITAL TO ANALOGUE CONVERTER USER GUIDE

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VISTEK V1624 digital to analogue converter

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1. OVERVIEW

The V1624 Precision 10 Bit DAC Module provides 10 bit precision conversion between a Component Serial Digital input signal to RGB or YPbPr output, 4 Serial Digital outputs as DAs and a separate Sync O/P is also provided.

Three auxiliary outputs are available. These may be configured as either an extra set of Y, Pb, Pr or three spare serial SDI outputs.

Remote control interface is available for communication between modules within the frame, and others outside it.

With the optional matrix board fitted, the unit can be configured to provide RGB output, or YPbPr with Betacam levels.

Full Specification CCIR 601 filters are used to ensure full compatibility and system integrity. A lower cost option is available using Near 601 performance filters.

2. MAIN FEATURES

- Full 10 Bit Precision
- Full Specification CCIR 601 Filtering
- User selectable configuration
- RGB or, with optional matrix board, YPbPr Outputs (N10 or Betacam levels)
- 4x Serial outputs



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3. INSTALLATION

3.1 Introduction

This section gives information on installing the V1624 DAC modules into the V1601 and V1603 interface frames and details on the connections that can be made to it. Information is also supplied on the function of each Preset adjustment and switch which are made available to the user on the front panel.

3.2 Installing Modules

The V1601 and V1603 frames are normally supplied with modules fitted. However, if further modules are to be fitted to a part-loaded unit, follow the instructions below.

3.3 Rear (I/O) Modules

Remove the screws from the blanking plate covering the spare position at the rear of the equipment and remove the plate. Place the new rear module in frame and slide into the unit until the connector(s) mates. The connector panel on the rear module should be seated flush with the rear cross extrusions of the frame when inserted correctly. Screw the module to the rear cross extrusions with the screws provided.

3.4 Front Modules

Unscrew the 2 captive screws at the top of the front panel of the frame and fold it down. Place the new front module in the card guides (take care to insert the circuit board into the runners and not the screen plate if fitted) and slide into the frame until it mates with the rear module. Close the front panel.

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3.5 Rear Panel Connections

All the input and output connections are available on the rear panel as shown below.

Serial Digital Input:
SD (IN)

This BNC connector is internally terminated with 75 Ohms.
The Serial Digital Input should be connected to this BNC.

Serial Digital Output:
SD1 (OUT)

Loop through output from SD (IN).

Serial Digital Outputs:
SD2 (OUT) - SD4 (OUT)

Serial digital outputs to SMPTE T14.22/082.

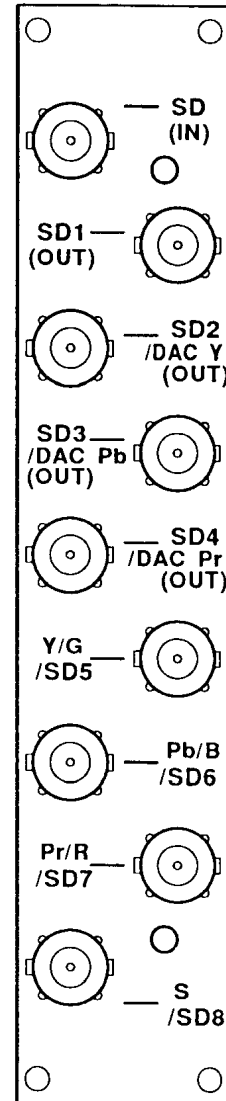
OR

Additional Y, Pb, Pr outputs, see SW5, SW6 & SW7.

Component Outputs/Digital Outputs:
Y/G/SD5, Pb/B/SD6, Pr/R/SD7.

Sync Output:
S/SD8

This is a separate sync supplied separately for component outputs.





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3.6 Front Panel Controls

A view of the front panel indicators and controls is shown below.

Front Panel Indicators

The **+V** lamp indicates that power is applied to the module.

The **REM** lamp indicates that the module/control system communications link is accessing the module.

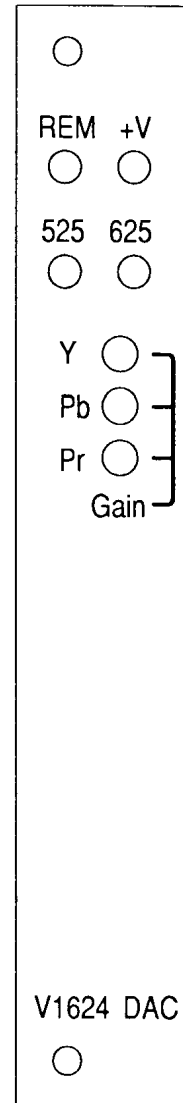
The **525** lamp indicates that the unit is working in 525 mode and is locked to 270 Bit/s serial digital input signal.

The **625** lamp indicates that the unit is working in 625 mode and is locked to 270 Bit/s serial digital input signal.

Front Panel Controls

3 variable resistors for gain output adjustment.

These adjustments are set at the factory. It is recommended that these are not adjusted without the correct monitoring/test equipment.



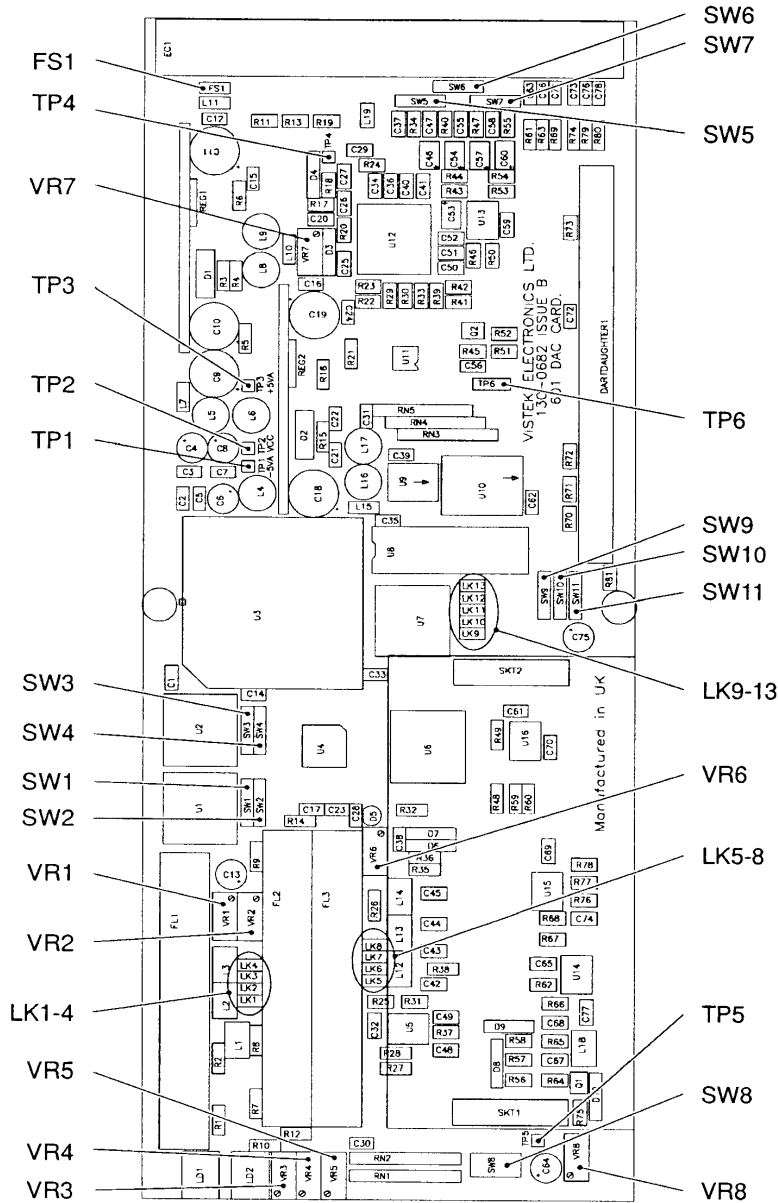
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3.7 On Board Controls & Adjustments

Locations of switches and Preset potentiometers are shown in the figure below.

To gain access to these controls and adjustments the board must be removed from the chassis. If the adjustments need to be made while the unit is powered up, an extender card needs to be used.



When reference is given to the direction / position of switch settings, it assumes that the module is in the vertical position as in the rack with its control panel on the left.



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Switch	Setting	Function
SW1	To the Rear To the Front	0 pixel delay added to Pb channel 2 pixel delay added to Pb channel
SW2	To the Rear To the Front	0 pixel delay added to Pb channel 1 pixel delay added to Pb channel
SW3	To the Rear To the Front	0 pixel delay added to Pr channel 2 pixel delay added to Pr channel
SW4	To the Rear To the Front	0 pixel delay added to Pr channel 1 pixel delay added to Pr channel
SW5	Up, b-c Down, a-b	Spare Y (N10) output Spare re-clocked SDI output
SW6	Up, b-c Down, a-b	Spare Pb (N10) output Spare re-clocked SDI output
SW7	Up, b-c Down, a-b	Spare Pr (N10) output Spare re-clocked SDI output
SW8/1	Off On	8 bit operation 10 bit operation
SW8/2	Off On	Black clip is enabled Black clip is disabled
SW8/3	Off On	Analogue blanking Digital blanking
SW8/4	Off On	VITC pass VITC blanked
SW9	To the Rear, a-b To the Front, b-c	Matrix sub-board output if fitted YPbPr output from main board
SW10	To the Rear, a-b To the Front, b-c	Matrix sub-board output if fitted YPbPr output from main board
SW11	To the Rear, a-b To the Front, b-c	Matrix sub-board output if fitted YPbPr output from main board

The following potentiometers are calibrated at the factory before delivery, the unit will need to be re-calibrated if the settings are altered (see calibration section).

Y,Pb,Pr DC offset adjustment.

VR1, VR2 and VR6 adjust DC offset of the Y, Pb and Pr channels respectively.

Y,Pb,Pr Gain Potentiometers

VR3, VR4, and VR5 adjust the gain of the Y, Pb, Pr channels respectively.

Deserialiser VCO centre frequency adjustment. (Test point TP4)

VR7 adjust for centre frequency on TP4 the deserialiser PLL voltage test point.

In addition, the links 1-8, listed below, are selected during factory test for correct chroma/luma timing.

Link Position	Function
LK1	3/4 pixel delay added to the Pb channel
LK2	1/2 pixel delay added to the Pb channel
LK3	1/4 pixel delay added to the Pb channel
LK4	No delay added to the Pb channel
LK5	3/4 pixel delay added to the Pr channel
LK6	1/2 pixel delay added to the Pr channel
LK7	1/4 pixel delay added to the Pr channel
LK8	No delay added to the Pr channel

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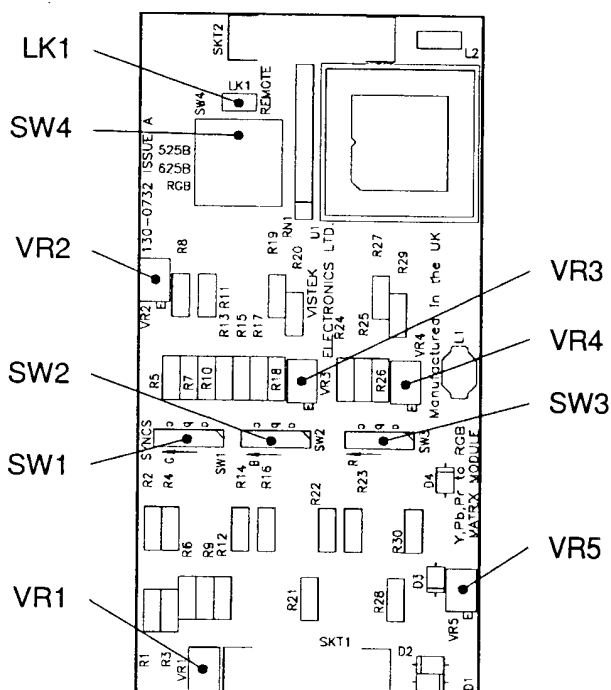
3.8 Matrix Sub-board

The matrix sub-board is designed to convert a Y, Pb, Pr component N10 level signal into an RGB output, it is also possible to by-pass the matrix section and provide the Y, Pb, Pr output signal at N10 or Betacam levels.

VR1 adjusts the Y gain for 525 Betacam level; Pb and Pr are not adjustable on the sub-board.

VR5 adjusts the pedestal on the 525 Betacam signal.

VR2, VR3 and VR4 adjust the G, B, R output levels.



Switch	Position	Function
SW1	b-c a-b	Syncs on Green in RGB mode No syncs on green
SW2	b-c a-b	Syncs on Blue in RGB mode No syncs on blue
SW3	b-c a-b	Syncs on Red in RGB mode No syncs on red
SW4-1	ON OFF	RGB outputs selected YpbPr outputs selected
SW4-2	ON OFF	625 Betacam YpbPr output level 625 N10 YpbPr output level
SW4-3	ON OFF	525 Betacam YpbPr output level 525 N10 YpbPr output level
SW4-4	ON OFF	Remote Control



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4. CALIBRATION OF V1624 DAC MODULE

4.1 Introduction

This section is intended to provide sufficient information to allow an engineer to calibrate the DAC system. Calibration should only be carried out if the unit has been mal-adjusted, or if drift has occurred over an extended period of time.

It should be appreciated that calibration is not a duplication of the alignment procedure, which should be referred to if a repair has been carried to the module.

4.2 Test Equipment

- 100 MHz dual channel oscilloscope.
- Tektronix TSG-42210 bit serial test signal generator.
- Tektronix WFM601i Serial signal analyser.
- Tektronix 1781 test set
- Digital multimeter
- Standard RS trim tool

4.3 Environmental

The calibration should be carried out at a nominal temperature of 20 degrees Celsius.

4.4 Test Equipment Connection

Connect the serial digital outputs of the TSG422 to inputs of the unit under test. Use cables of the same type and equal length (this is necessary for luma-chroma delay calibration).

Connect one of the serial digital outputs from the unit under test to the VFM601i via a cable clone. Initially set the cable clone to zero metres.

Connect the Y Pb, Pr outputs of the unit under test to TEK1781 set.

4.5 Calibration Procedure

Initial Set-up: Ensure the following switches are set as detailed before starting calibration.

Switch	Setting	Function
SW8-1	ON	10 bit operation enabled
SW8-2	ON	Black clip disabled
SW8-3	ON	Digital blanking enabled
SW8-4	ON	Vertical interval data blanked
SW5, 6, 7	a-b	Auxiliary outputs configured of SDI
SW9, 10,11	b-c	Main outputs configured for YPbPr (N10/SMPTE)

4.6 Power Distribution Check

Using a Digital Multi Meter, check the following points for the specified dc potentials:-

TP2 +5V +/- 0.2 V VCC

TP3 +5V +/- 0.2 V P5V A

TP1 -5V +/- 0.3 V N5VA

TP6 may be used as the ground reference

Serial input: re-clocking and de-serialisation

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4.7 Clock Centre Frequency Calibration

Set the TSG422 generator to provide the SDI matrix check field.

Whilst monitoring the 601i and TP4 (oscilloscope) adjust VR7 (VCO centre frequency) until lock is achieved without data errors. A method for setting the VCO centre frequency is described in the Gennum 1994 Data book (page 2-47):

"Tune the potentiometer (VR7) so that the PLL loses lock at the low end (lowest loop filter voltage at TP4). Increase the potentiometer slowly until the loop re-locks. Record the loop filter voltage at this point as Vcl. Now adjust the potentiometer (VR7) so that the loop filter voltage (TP4) is 200mV above Vcl."

Remove and then re-apply the serial input signal. Confirm that the card re-locks.

4.8 Y, Pb, Pr DC Offset Adjustment

Set the TSG422 generator to provide 625 100% colour bars.

Monitor the Y output using the oscilloscope.
Adjust VRI for a dc offset of 0V +/- 10mV on the displayed signal.

Monitor the Pb output using the oscilloscope.
Adjust VR2 for a dc offset of 0V +/- 10mV on the displayed signal.

Monitor the Pr output using the oscilloscope.
Adjust VR6 for a dc offset of 0V +/- 10mV on the displayed signal.

4.9 N10/SMPTE Level Adjustment (including syncs)

Set the TSG422 generator to provide 625 100% colour bars.

Monitor the Y output using the 1781 measurement set. Adjust the front panel Y gain control pot (VR3) for an amplitude of 700 mV black to peak white.
Adjust the syncs amplitude pot (VR8) for 300 mV p-p of syncs.

Monitor the Pb output using the 1781 measurement set. Adjust the front panel Pb gain control pot (VR4) for an amplitude of 700 mV peak to peak.

Monitor the Pr output using the 1781 measurement set. Adjust the front panel Pr gain control pot (VR5) for an amplitude of 700 mV peak to peak.

Set the TSG 422 generator to provide 525 100% colour bars.
Check that the Y, Pb, Pr levels have not deviated from those set above.

This completes the V1624 DAC Module calibration.