CIFER
CIFER/SD
HD Standards Converter

User Guide

Issue: 2.0

www.pro-bel.com

Contents

1 Description

Cifer is a very high quality Frame Rate Standards Converter for use in any broadcast installation that processes High Definition video signals. It uses advanced signal processing techniques to achieve the very highest quality of video when converting between standards with different frame rates. So that Cifer can be used in many broadcast installations that have to handle a wide variety of standards; it can also convert between standards of the same frame rate. This makes it a device that can provide outstanding pictures from a source of almost any standard, and as well as providing frame rate conversion it also replaces Up, Down and Cross Converters and in some cases Aspect ratio Converters.

Since some installations do not need to produce High Definition (HD) there is an economical version of the converter, Cifer/SD, which can only produce Standard Definition (SD) signals on its output. This version can still process HD signals on its input, but can only produce SD output signals. This could be used, for example, in a SD play out facility where the input signal could be any standard but only an SD output is needed. In this type of application Cifer/SD can replace the need for separate SD Frame Rate, Up and Down converters.

Cifer and Cifer/SD are both a part of the Vistek V1600 range of modular products. Unlike some of the simpler modules in the range there are two physical processing modules; one provides the video interfacing, processing and control, while the other provides the real time Motion Estimation needed for the Frame Rate Conversion. Each one of these cards needs a fan card beside it to maintain the necessary temperature operating range, so that a basic Video Cifer occupies four slots in the standard Vistek V1606 Frame. It is therefore possible to fit three Cifers in a 3U rack and still have two spare positions.

An optional Audio Processing card, the V6302, is also available. While this is an independent module in its own right it can be fitted immediately next to the Cifer modules, with a shared passive rear module, so that there is tight coupling between them. For example embedded digital audio can be extracted from the input video, processed (which might include decoding of Dolby E surround sound) and then embedded onto the output video. In particular the audio is delayed so as to maintain lip-sync with the video.

Cifer also handles many other forms of auxiliary data, such as Closed Captions, Source Identification and Time Code.

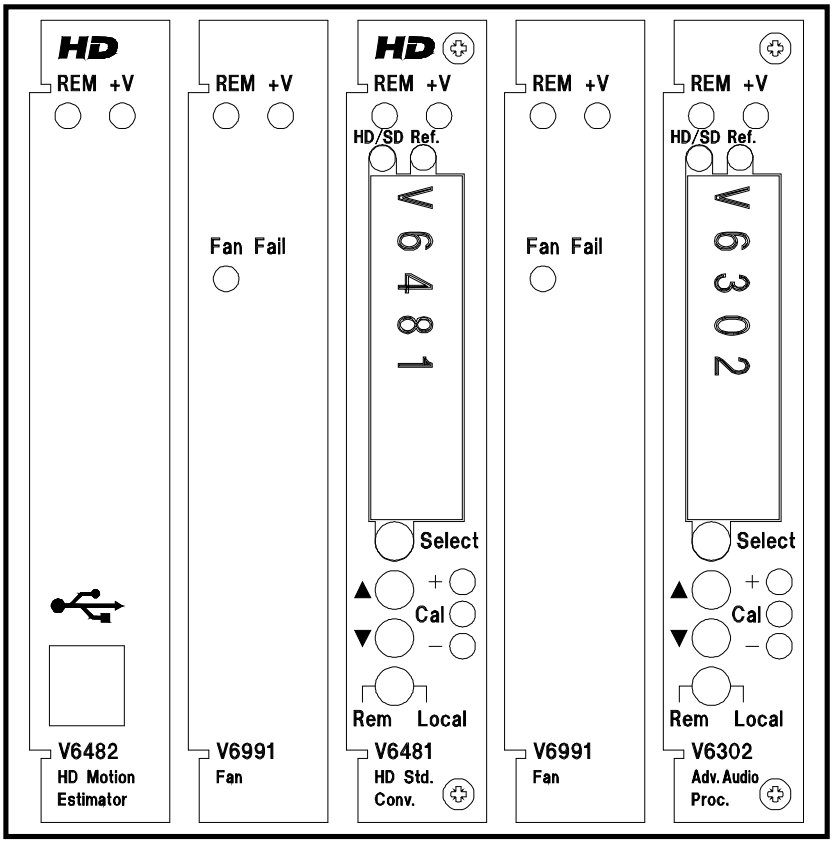
For the rest of this document any reference to CIFR also applies to Cifer/SD unless explicitly stated otherwise.

2 Installation

2.1 Assembly

Cifer normally occupies five slots in the V1606 Frame, which includes the V6302 Advanced Audio Processing module.

They modules in the group should be mounted into the rack as shown here:



The rear module must be fitted before any of the main modules can be inserted.

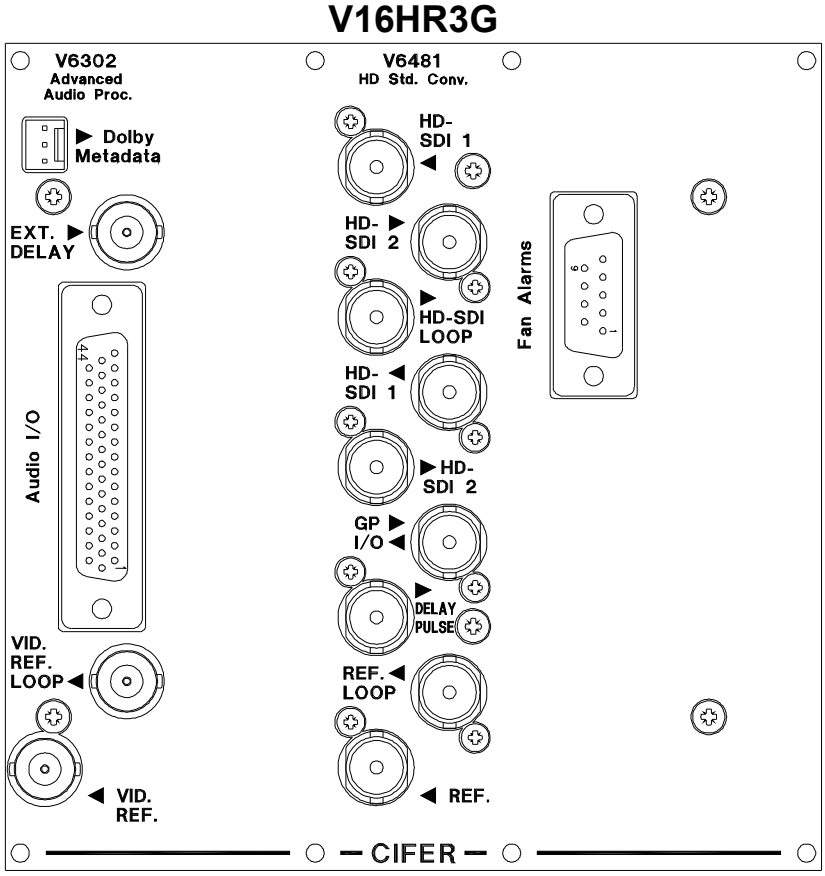
For normal operation it is important that both Fan modules, V6991, are fitted. However for short periods, say up to about 5 minutes in a normal working environment Cifer can be operated without one or the other fans. This could be useful in the case of the fans being replaced during maintenance.

As with all V1606 Modular Frame installations the modules should be distributed evenly across the fourteen available slots to satisfy the cooling requirements. Clearly this does not apply within the Cifer group of modules, but any other modules in the frame should follow this recommendation. If there are spaces in the frame then they should generally be on the

left, when viewed from the front, and not on the right near the Power Supplies.

2.2 Rear Panel

This drawing shows the **rear view** of the V16HR3G five position Rear Panel for Cifer. This includes the position for the V6302 Advanced Audio Processing module.



2.3 Connections

2.3.1 Video Connections

This table describes the video connections labelled under V6481.

Connector	Type	Function
► HD-SDI 1	BNC	Serial Digital Video Input 1. Can be either SD or HD.
► HD-SDI 2	BNC	Serial Digital Video Input 2. Can be either SD or HD.
◄ HD-SDI LOOP	BNC	Serial Digital Video Output from selected Input. Can be either SD or HD. It is buffered and Reclocked from the input, but is **not** converted. Can be either SD or HD

◄ HD-SDI 1	BNC	Serial Digital Video Main Output 1. Can be either SD or HD on Cifer, but only SD on Cifer/SD.
◄ HD-SDI 2	BNC	Serial Digital Video Main Output 2.Can be either SD or HD on Cifer, but only SD on Cifer/SD.
► ◄ GP I/O	BNC	General Purpose Input or Output (bi-directional)
◄ DELAY PULSE	BNC	Delay Pulse Output. This is a 'TTL' type logic pulse whose positive portion represent the Video delay being inserted.
◄ REF. LOOP	BNC	Passive loop Output from Reference Input (below). This is a hard connection on the rear panel, so remains even if the main board(s) is removed.
► REF.	BNC	Video Reference Input. This can be either a conventional bi-level sync or composite video signal, or a modern tri-level sync signal. A 75Ω termination can be applied using a small switch on the V6481, but it will be removed if the board is removed.

2.3.1 Audio Connections

This table has the connections to the V6302 audio card. Some connections are not usually used in the Cifer application because their function is applied internally, but they are included here partly for completeness, as they are available on the rear panel, but also so that the V6302 could be used independently of the Cifer video functions.

Connector	Type	Function
► Dolby Metadata	Molex 3 pin	Serial Metadata from Dolby Decoder. The Dolby Decoder is an option on the V6302.
► EXT. DELAY	BNC	TTL pulse input from an external device to set the audio delay. Not used in Cifer.
► ◄ Audio I/O	44 way HDD	All audio I/O. See below for contact details.
◄ VID. REF. LOOP	BNC	Video Reference Loop Output for the Audio Processor
► VID. REF.	BNC	Video Reference Input. This can be either a conventional bi-level sync or composite video signal, or a modern tri-level sync signal. Used for the Audio Processor. A 75Ω termination can be applied using a small switch on the V6302, but it will be removed if the board is removed.

This table defines the connections to the 44 way High density D-type connector. It is given here for completeness, but for full details the manual for the V6302 should be used.

Signal Group Label	HDD44 Pin	Signal Function
Audio 1 AES A ⇐	14	Input AES A Pos
	44	Input AES A Neg
	15	Input AES A Gnd
Audio 2 AES B ⇐	13	Input AES B Pos
	43	Input AES B Neg
	28	Input AES B Gnd
Audio 3 AES C ⇐	12	Input AES C Pos
	42	Input AES C Neg
	26	Input AES C Gnd
Audio 4 AES D ⇐	11	Input AES D Pos
	41	Input AES D Neg
	40	Input AES D Gnd
Audio 5 AES E ⇐	9	Input AES E Pos
	39	Input AES E Neg
	10	Input AES E Gnd
Audio 6 AES F ⇐	8	Input AES F Pos
	38	Input AES F Neg
	24	Input AES F Gnd
Audio 7 AES A1 ⇒	7	Output AES A1 Pos
	37	Output AES A1 Neg
	21	Output AES A1 Gnd
Audio 8 AES A2 ⇒	6	Output AES A2 Pos
	36	Output AES A2 Neg
	5	Output AES A2 Gnd
Audio 9 AES B1 ⇒	4	Output AES B1 Pos
	34	Output AES B1 Neg
	19	Output AES B1 Gnd
Audio 10 AES B2 ⇒	3	Output AES B2 Pos
	33	Output AES B2 Neg
	19	Output AES B2 Gnd
Audio 11 AES C1 ⇒	2	Output AES C1 Pos
	32	Output AES C1 Neg
	16	Output AES C1 Gnd
Audio 12 AES C2 ⇒	1	Output AES C2 Pos
	31	Output AES C2 Neg
	16	Output AES C2 Gnd

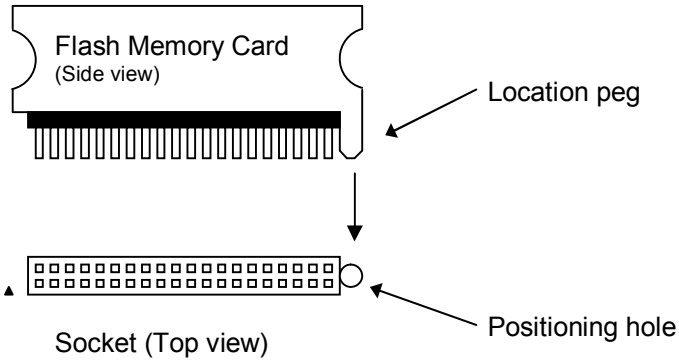
Audio 13 AES D1 ⇒	23	Output AES D1 Pos
	22	Output AES D1 Neg
	35	Output AES D1 Gnd
Audio 14 AES D2 ⇒	18	Output AES D2 Pos
	17	Output AES D2 Neg
	35	Output AES D2 Gnd
AES Ref 1 AES REF ⇐	20	AES REF input Pos
	25	AES REF input Neg
	29	AES REF input Gnd
Misc EXT. DELAY ⇐	30	Ext. Delay pulse input
	29	Ext. Delay pulse GND
	27	

Note:

1. Pin 1 is at the bottom
2. The HD44 connector provides only balanced inputs and outputs.

2.3.2 Flash Memory Card

The Flash Memory Card stores the firmware for the Micro-controller and the FPGA and is essential for the operation of the module. If this card is missing, the front panel display will come up with an error message (ERROR 10). The Flash Memory Card sits in a socket with a location peg to the right. In case of a firmware upgrade, one has to make sure that the replaced card sits firmly and straight in the socket with the location peg mating with the positioning hole on the baseboard.



The Flash Memory Card is re-programmable. Customers are kindly asked not to throw it away after having upgraded a module with a newer firmware version. A Vistek service technician will collect it on his/her next visit or it can be put in an envelope and sent back to the postal address shown on the cover of this manual.

3 System Operation

3.1 Local Control

3.1.1 Start Up

Local control and monitoring of the module is done through the front panel with its eight character LED display and three control buttons **Select**, ▲ and ▼. There are three LEDs which also contribute to the status indication; these are labelled **+**, **Cal** and **–**.

After power up and having successfully passed the power-on-self test, the display will start at the top level and show the unit type and any options that are included. The display will be one of these:

Unit type	Password protected Option(s)
CIFER	SD

3.1.2 Option Abbreviations

Options are indicated by abbreviations. The following list illustrates their meanings:

Option	Meaning
SD	**S**tandard **D**efinition output only unit.

3.1.3 Menu Control

The **Select,** ▲ and ▼ buttons are used to manoeuvre around the menu system. The menu structure has five levels and the **Select** button is used to go up and down the structure. The ▲ and ▼ buttons are used to move between selections or to adjust a parameter depending on which sort of menu is displayed. The five levels are as follows:

Sleep	Display is blank (except for Banner warnings).
Top Level	As above, e.g. **CIFER**
Main Menu	The Main menu items, such as **VIDEO**, **STATUS**, **ENG'ING** etc. These items are all in Upper Case.
Sub Menu	Menu items under each main heading, such as **Source** or **O/P LStd** under the **VIDEO** main menu. These items are all in Sentence Case (generally lower case but with upper case first letters).
Parameter	The lowest level under the Sub Menu, and used to actually adjust a parameter. The display will depend on the actual parameter and may be a value such as **+0.00dB** for a gain or **ON** or **OFF** for a switch variable. There is usually a title to describe the variable and a small icon in the left hand character position, but 8 characters cannot provide for a detailed description.

To move down a level just press the **Select** button briefly; then press either the **Select** button again to go down another level or the ▲ and ▼ buttons to move around the options within a level.

To move up a level press and hold the **Select** button for about half a second which will move up one level. If you continue to hold the **Select** button then it will move up a level every half a second until it reaches the Sleep level (one above the Top Level).

A complete list of all the menus is given in Section 5.

3.1.4 Menu Examples

This section has examples of how to manoeuvre through the menu system. The first one starts with the unit in its 'sleep' mode where the display is blank, and then proceeds to set the reference source to the processing input (*Vid I/P*).

Action	Display	Comments
Select	**CIFER**	Top Level
Select	**VIDEO**	The Main Menu we want
Select	**Source**	The first Sub Menu in the list
▼	**O/P LStd**	
▼	**O/P FldR**	The Sub Menu we want
Select	**Auto**	The default setting
▲	**50Hz**	Set it as we want it

3.1.5 Sleep

If the front panel is not used for a certain amount of time then the display will automatically go into a sleep mode when it will be blank. Pressing any of the buttons will cause it to 'wake up' back into the top level. The time delay before the unit slips into sleep mode can be set up using the **CONFIG** : **Sleep** menu.

The brightness of the display can also be adjusted using the **CONFIG** : **LEDLevel** menu.

3.2 Core Product Features

3.2.1 SDI Inputs

The SDI inputs must conform to either the SMPTE292M or SMPTE259M standards, which describe the Bit Serial Digital Interface for HD and SD operation. If only one input is required then it should be connected to SDI 1. Unused inputs can be left open, it is however recommended to terminate unused inputs with a 75Ω Terminator to improve noise immunity. Signals of different frame-rates, resolutions or even a mixture of SD and HD standards can be connected to both Inputs at the same time, however only one of the two inputs can be selected at a time. Note that switching between different standards is neither instant nor glitch-free. This has to do with the necessity of the SDI de-serialiser hardware to lock to the newly detected standard. Furthermore, in case of an SD-to-HD switch over (or vice versa), the FPGA on the baseboard must be re-loaded. This process takes about 2 to 3 seconds.

The input selection is done on the **VIDEO** : **Source** menu.

3.2.2 SDI Reclocked & Buffered Output

This is always available, and is a re-clocked version of either SDI 1 or SDI 2, depending on the source selection. It is an unprocessed signal, i.e. neither synchronised nor converted.

3.2.3 SDI Main Outputs

The main synchronised/processed SDI output is available on two BNCs.

3.2.4 Video Reference

The external video reference is available for units with the Frame Synchroniser function; it can be either a standard composite black and burst video signal, or a new style tri-level sync. The unit will automatically detect which and extract the relevant timing information.

The reference is looped on the rear module so it can be daisy chained along several modules. For accurate timing, this is not recommended. There is a termination on the I/O daughter module, which can be switched in at the end of the chain. Care should be taken to ensure that each reference has only one termination set.

The units can operate from either the external reference or use the selected SDI input. This is selected on the **TIMING** : **Ref Src** menu. When set to *Auto*, the external reference will be used if available; otherwise the selected SDI input will be used as the reference.

3.2.5 Standard Detection

The units detect and report back the detected video standard and frame-rate of the selected SDI input and that of the reference input. The detected standard can be seen in the **STATUS** menu under **I/P Std** and **Ref Std**.

3.2.6 TRS Signals

The TRS signals are the digital equivalent of the analogue synchronising pulses. All modules described in this manual always regenerate the TRS signals on their output, so that any errors on the input signal will not be propagated through.

3.2.7 EDH (SD operation only)

EDH is a method of embedding data within the ancillary data space that carries a measurement of the integrity of video and other data. By regenerating the equivalent measurement at the receiving end it is possible to check that the data has been received correctly.

HD signals always have the EDH data in form of checksums embedded, but for SD signals it is optional. On Cifer the EDH on the output can be disabled on the **ENG'ING** : **O/P EDH** menu. Care must be taken if the new EDH generation is disabled and the old EDH is being passed through because it will probably not correctly represent the data. In this case the Ancillary Data really ought to be blanked.

3.2.8 Illegal Codes

A function of these modules is to ensure that the SDI output always meets the relevant specification. In particular this means that the output is always legal in the sense of Line Length, Field Length and data values. In the main this works extremely well, but there are some circumstances where it fails:

- If the output timing is being changed, there will be momentary errors.
- If the input is noisy, such that erroneous data is received, then the ancillary data may get checksum errors. This obviously only applies if the Ancillary data is being passed. The video will be all right, since the EDH (SD operation), respectively the line numbers and CRC codes in accordance with SMPTE 292M (HD operation) are regenerated on the output.
- If the reference is unstable or changing standards then the output will not be stable.

3.2.9 VCO Centre Frequency

Normally, the output is locked to the video reference - if present - and of the same standard as the video, or to the input video itself. If there is no signal or reference connected then the output will free run at the nominal centre frequency of the on board clock generator. This centre frequency can be adjusted under the **CALIB** : **CntrFreq** menu, but this should not normally be necessary in the field.

It is possible to force the unit into its free-run mode using the **ENG'ING** : **Free-run** menu. This is an unusual requirement and so is a setting that appears on the top-level banner when set.

3.2.10 Version Numbers

The Cifer module comprises various items of software/hardware and they all have separate version numbers. These can be read on the following read only menus:

VERSION	**PROM Ver**	03.00	PROM stick version
	MEC Ver	2.20	V6482 software version
	Soft Ver	05.01.00	Versions of software / firmware / hardware components.
	Boot Ver	02.00.00	
	Strx Ver	1.4.00	
	FPGA Ver	01.04	
	CPLD Ver	00.01	
	Data Ver	29000002	
	PCB Ver	00.00	
	VPModule	ᴹHD PROC	
	IOModule	STD [3]	

3.2.11 Display Sleep

Since, for the vast majority of its life, a module will operate behind the front panel of a rack frame, the display on the local front panel will not be visible so it will go to sleep after a certain time. This timeout delay can be changed on the **CONFIG**:**Sleep** menu to be anything between 0 and 30 minutes; 0 minutes means that it will stay on indefinitely. The sleep timeout always counts from the last front panel button push. The default time is 5 minutes.

The panel can also be forced into its sleep mode by moving up a level from the Top Level menu, which displays the module type.

To get the display to come on again simply press one of the buttons and the menus will start again at the Top Level.

3.2.12 Display Brightness

The brightness of the front panel display can be adjusted on the **CONFIG**:**LEDLevel** menu.

ENG'ING LEDLevel ▓ ▓ ▓ ▓

3.3 Output Format and Aspect Ratios

3.3.1 Output Line and Frame Rate

The output format is selected using two controls; one of these, **VIDEO** : **O/P LStd** , controls the line standard e.g. 720 or 625, the other, **VIDEO** : **O/P FldR** selects the field rate for example 50 or 59.94.

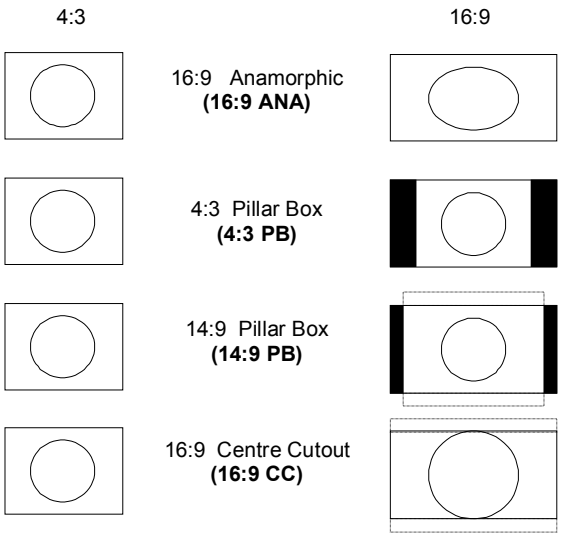
These controls have the following available settings:

		O/P FldR		
		Auto	50	59.94
O/P LStd	Vid I/P	ü	ü	ü
	525i	ü	X	ü
	625i	ü	ü	X
	1080i	ü	ü	ü
	720p	ü	ü	ü

When these controls are set to the 'Vid I/P' or 'Auto' settings the input is used to select the output line standard or frame rate. If an illegal combination is selected then a flashing ▒ symbol will appear to the right of the selected field rate or line standard on the front panel.

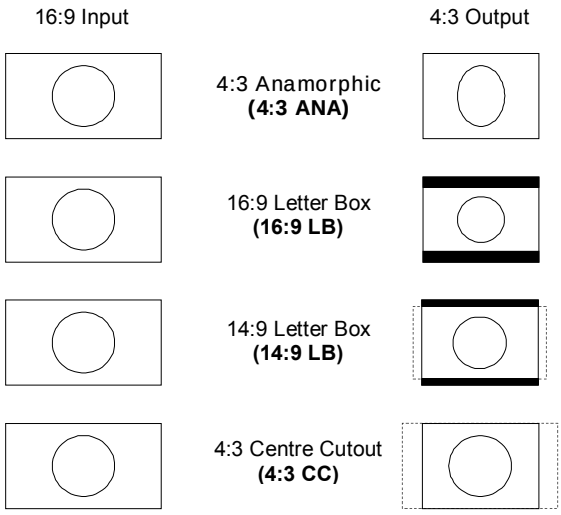
3.3.2 Up-Conversion

When up-converting, i.e. taking in an SD output either 525 or 625 and converting to an HD output, the aspect ratio is controlled by the **VIDEO** : **A/R Up** menu, which has the following options :



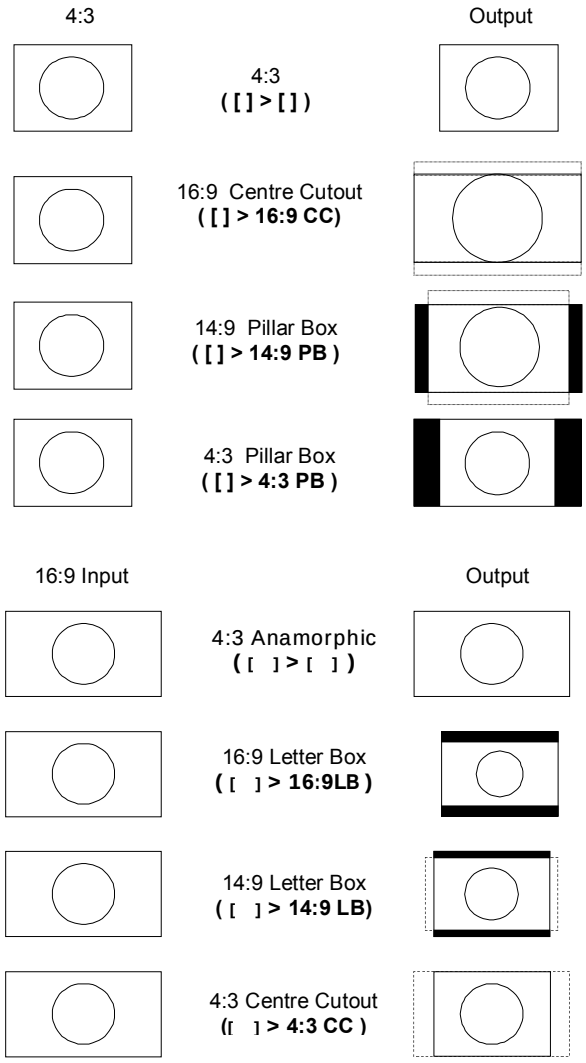
3.3.3 Down Conversion

Cifer gives four down conversion options in the **VIDEO** : **A/R Down** menu. They are shown diagrammatically below. Note that some conversion settings result in a loss of parts of the original picture (indicated by dotted areas).



3.3.4 SD Aspect Ratio Conversion

When converting between SD standards, there are 8 available preset aspect ratio conversions. These can be found in the **VIDEO : A/R SD>SD** menu. These are described in the diagram below.



3.3.5 SD Width Control

In a digital SD signal there are 720 luminance samples in an active line which equates to 53.33us in the analogue world. A true PAL signal has an analogue line length of 52us, which equates to 702 luminance samples in the digital domain, and NTSC has an analogue line length of 52.66us equating to around 711 luminance samples.

In HD standards the line length is always considered to be the full digital line.

When converting between HD and SD, there is some ambiguity about how images should be scaled. Should the whole HD line be scaled to the whole digital SD line, or the slightly shorter analogue dimension? A control has been provided, **VIDEO : SD Width,** which allows the user to choose which option to use. This control has the options *SDwd Ana* and *SDwd Dig*, referring to analogue and digital SD widths. When set to analogue, the unit will scale images as if the SD line was the shorter analogue length. When set to digital, the SD line will be considered to be 720 samples long.

3.3.6 Down Conversion Resolution Controls

When down converting, the source material is of much higher resolution than the output as a result some fine detail must be lost. In the default mode of operation the unit will preserve as much picture information as it can, giving a very sharp output picture. The resultant image can look too sharp for some purposes, especially in the vertical direction where high-resolution detail can be seen as flickering. For this reason two controls have been provided, **ENG'ING : H Res** and **ENG'ING : V Res**; these control the horizontal and vertical resolution of the output when down-converting, and have the options *high, medium* and *low*. The *high* setting passes the most detail, and *low* is the softest.

3.4 Output Timing, Reference and Frame Synchroniser

3.4.1 Timing & Delay Control

3.4.1.1 With External Reference (Ref I/P)

If an external, analogue Reference signal (e.g. Bi- or Tri-Level Sync) of the same frame rate as the output is present *and* the reference source selection control (**`TIMING`** : **`Ref Src`**) is set to *Auto* or *Ref I/P*, Cifer will automatically ensure the output is frame synchronous to the analogue reference input.

Depending on whether the unit is doing a frame rate conversion, the behaviour when locking to the reference alters slightly:

When frame rate converting, e.g., converting from 50 to 59.94Hz, the unit has a fixed video insertion delay of 200ms, irrespective of the reference phase, or any timing adjustments made with respect to the reference. When the output timing is adjusted, the temporal video processing keeps the delay at 200ms.

When the unit is not frame rate converting, i.e. input and outputs are the same frame rate, the insertion delay of the unit is 200ms + 0-40ms synchronisation delay. This will be dependent on the relative timing of the input and reference, and any offset timing applied relative to the reference. The extra delay being added on top of the units fixed 200ms insertion delay is reflected on the delay pulse output.

In order to keep alignment with the incoming SDI data, the Frame-Synchroniser will either repeat a frame or drop a frame once in a while, depending on a) which of the two clock domains (Input Video versus Reference signal) is the faster, and b) how far the two clock domains are apart (typically in the range of 0 to ± 150ppm).

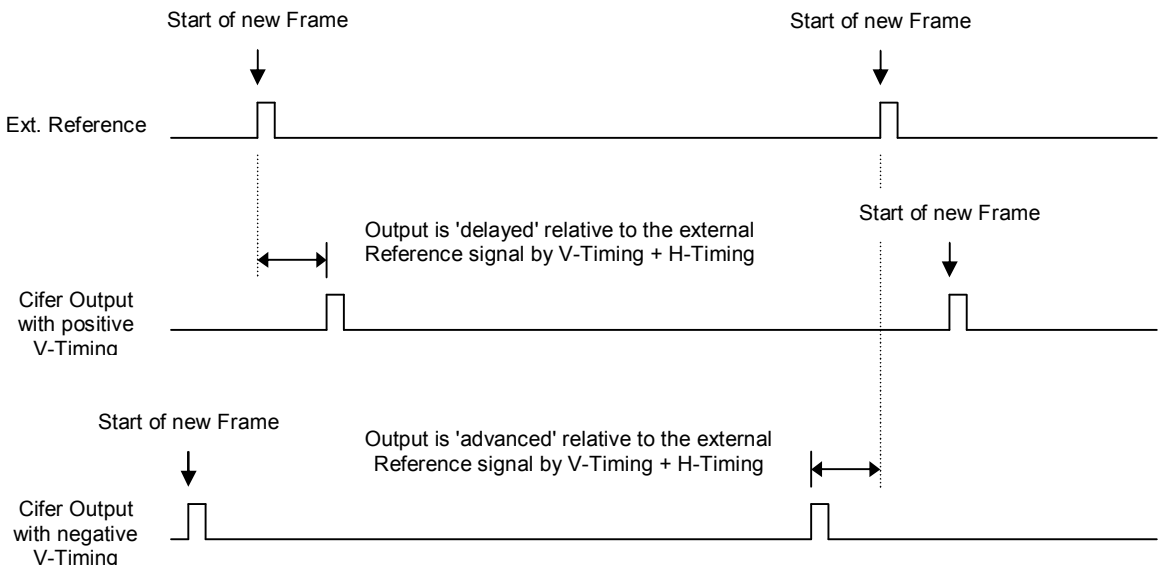
When operating Cifer locked to an analogue reference, two timing controls (V- & H-Timing) are available for adjusting the board's output timing relative to the external Reference signal.

`TIMING` : **`V Timing`**: Purpose: For vertical adjustment (in number of lines)

Range: -256..+255 lines

`TIMING` : **`H Timing`**: Purpose: For horizontal adjustment (micro seconds)

Range: 0µs up to one line (one pixel resolution)



This drawing illustrates the **Reference-to-Output** timing relationship when operating Cifer locked to an external analogue reference.

Note that the Input-to-Output delay when the unit is not frame rate is variable and spans from a minimum delay up to a complete Frame. This timing variation can be monitored on the Delay Pulse BNC.

3.4.1.2 With Internal Reference (Vid I/P)

When it is not converting frame rates, Cifer can be used as a straightforward, adjustable delay module, in applications where for example the incoming SDI signal is already frame-synchronous but requires an arbitrary delay.

Disconnecting the external Reference signal (in case **VIDEO** : **Ref Src** is set to *Auto*) or forcing the unit to take its Video Input as the Reference signal (**VIDEO** : **Ref Src** is set to *Vid I/P*) will automatically disable the Frame Synchroniser function and put the board into a pure delay mode.

It should be noted that the unit cannot lock to the video input when a frame rate conversion is taking place, so the unit will free-run if the SDI input is selected as the reference source.

When locking to the SDI input, the H- and V-Timing controls are hidden, and H- and V-Delay controls appear in the TIMING menu. These are different controls, and there values are stored separately.

Important:

If **VIDEO** : **Ref Src** is set to *Auto* and no external Reference signal is present, the unit assumes that there is a persistent problem with the external Reference and the actual insertion delay is controlled by the setting in the **VIDEO** : **RFL Mode** menu:

If **RFL Mode** is set to *Min Dly*, all delay control settings will be forced to zero and the unit continues operating in a minimum delay (= intrinsic delay) mode.

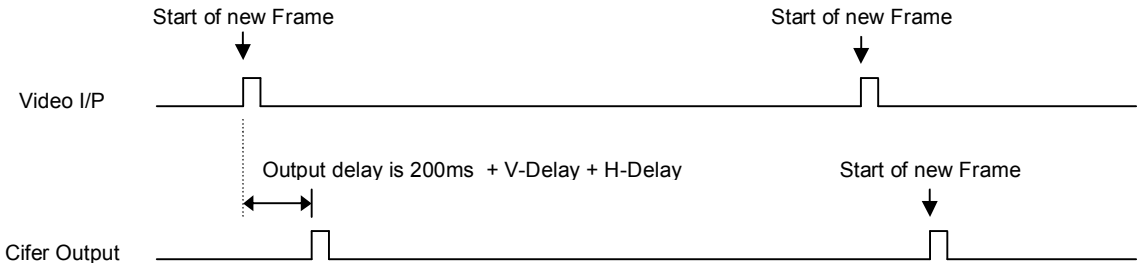
If **RFL Mode** is set to *Adj Dly*, the insertion delay is the sum of the unit's intrinsic delay plus whatever is set in the F-, V- and H-Delay controls.

VIDEO : **V Delay**: Purpose: Fine delay (in number of lines)

Range: 0 up to (number of total lines per field/frame – 1 line)

VIDEO : **H Delay**: Purpose: Super fine delay (in microseconds)

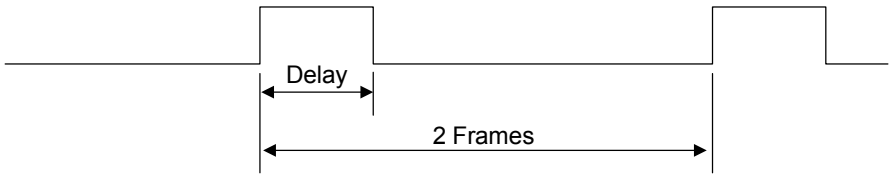
Range: 0µs up to (duration of one line – one pixel)



3.4.2 Delay Pulse

The Frame Synchronizer produces a signal that represents the variable delay being inserted into the video path. This delay information is passed on internally to the V6302 Advanced Audio Processor (if present) and used to provide a tracking delay to the audio. The signal is also available externally so it can be used by other audio tracking devices. Please note that the length of the tracking delay pulse is a measure for the variable delay between input and output only – it does not cover for any additional processing delay added on top of the variable delay.

The Delay signal has repetition rate of two frames and the positive pulse width represents the variable delay. This is shown in this diagram.



The external Delay Pulse output is available on a BNC on the rear panel. The external pulse itself is nominally 3.3V with a sourcing/sinking capability of ±24mA.

When no extra delay is being added on top of the standard 200ms delay, the delay pulse will reduce to its minimum width of 10us.

3.4.3 Video Reference Fail

When there is no external reference signal present, and the unit is not frame rate converting, the unit will lock to the SDI input. When frame rate converting the unit cannot lock to the input, and so will free-run if no usable reference is supplied.

Under the circumstances described above and depending on the setting of **VIDEO** : **RFL Mode** (**R**eference **F**ail **Mode**), the module then switches automatically into a minimum delay mode (*Min Dly*) or it maintains the delay set by the F-, V- and H- Delay controls (*Adj Dly*).

With same frame rate conversions, a module can be also forced to use the SDI input as its timing reference by setting **VIDEO** : **Ref Src** to *Vid I/P*. In this case, the current setting in **VIDEO** : **RFL Mode** will be ignored and the total insertion delay simply depends on the current settings in the F-, V- and H- Delay controls. When frame rate converting the unit cannot lock to the input, so will free run.

3.4.4 Video Reference Mismatch

When a mismatch between the Video Output's frame-rate and the Reference's frame-rate is being detected, if the unit is frame rate converting, the output will free-run. Otherwise the unit will lock to the video input.

3.5 Video Processing Amplifier

3.5.1 Video Gain

PROC AMP V Gain

The adjustment range is ±6dB and it applies equally to the luminance and both of the chrominance channels (Cb and Cr). The gain is applied after the black level offset. The Video gain is applied simultaneously with the Chrominance gain so they can cancel one another out. For example +3dB of Video gain along with –3dB of Chroma gain will result in the luminance being increased by +3dB and the Cb and Cr channels being unchanged.

The output is limited to ensure that there is no numerical overflow as the output fits into the 10 bit D1 domain. There is no gamut legalisation function.

3.5.2 Chroma Gain

PROC AMP C Gain

The adjustment range is ±6dB and it applies equally both the chrominance channels. The gain is applied along with the video gain and after the black level offset. The Chrominance gain is applied simultaneously with the Video gain so they can cancel one another out. For example +3dB of Video gain along with –3dB of Chroma gain will result in the luminance being increased by +3dB and the Cb and Cr channels being unchanged.

The output is limited to ensure that there is no numerical overflow as the output fits into the 10 bit D1 domain. There is no gamut legalisation function.

3.5.3 Black Level

PROC AMP Blk Lvl

The adjustment range is –127 and +128 D1 levels (equivalent to -101/+102mV). The black level adjustment is applied before the gain stages. This is considered the best arrangement since the unit is usually used to correct incoming errors.

3.5.4 Hue Shift

PROC AMP Hue

The adjustment range of the hue shift is ±45° in 0.35° steps.

3.5.5 Dynamic Rounding

PROC AMP Dyn Rnd

Since some quantising effects may be visible on the output of this unit when variable gains are applied, Dynamic Rounding has been applied. This Dynamic Rounding is only used to reduce the effects of the fractional bits of lower significance than the normal 10 bits; it does **not** reduce the resolution to 8 bits.

This can be disabled on the **PROC AMP** : **Dyn Rnd** menu.

3.5.6 Limiting

PROC AMP Hrd Clip

Since gain can be applied to the D1 signal it is possible to generate levels outside the normal 10 bit gamut of D1 and so limiting is required. The Proc Amp normally applies a soft form of limiting that progressively reduces the gain of a signal as it approaches the limits, either overshoot or undershoot. If this is not required then it can be disabled on the **PROC AMP** : **Hrd Clip** menu.

The limiting that is applied is 'simple' in that it does not ensure that the output is correctly within the colour gamut, but only that each of the three components (Y, Cb, Cr) remains within the legal 10 bit range.

Certain test patterns, most notable the amplitude ramps, contain data that is within the overshoot and undershoot areas. If they are passed through the Proc Amp with its default soft clipping then they will be modified. This means that the EDH value on the output will be different to that on the input. If this is not wanted then the Hard Clipping can be turned ON, but this is not recommended for normal Proc Amp operation.

3.5.7 Fade to Black

PROC AMP Fade>Blk

This enables the output to be cleanly attenuated to digital black on receipt of an internal command.

The rate of the fade is fixed at half a second.

Locally the fade can be initiated on the **PROC AMP** : **Fade>Blk** menu. This contains both an ON and OFF command.

The fade can also be initiated over the DART remote control network. The fade will start as soon as the command is sent.

The output will stay at black until any active control input is released, or the unit is reset. There is no direct indication on the front panel that the output is being forced to black except for the top level banner, if enabled.

3.6 Time Code and Source Identification

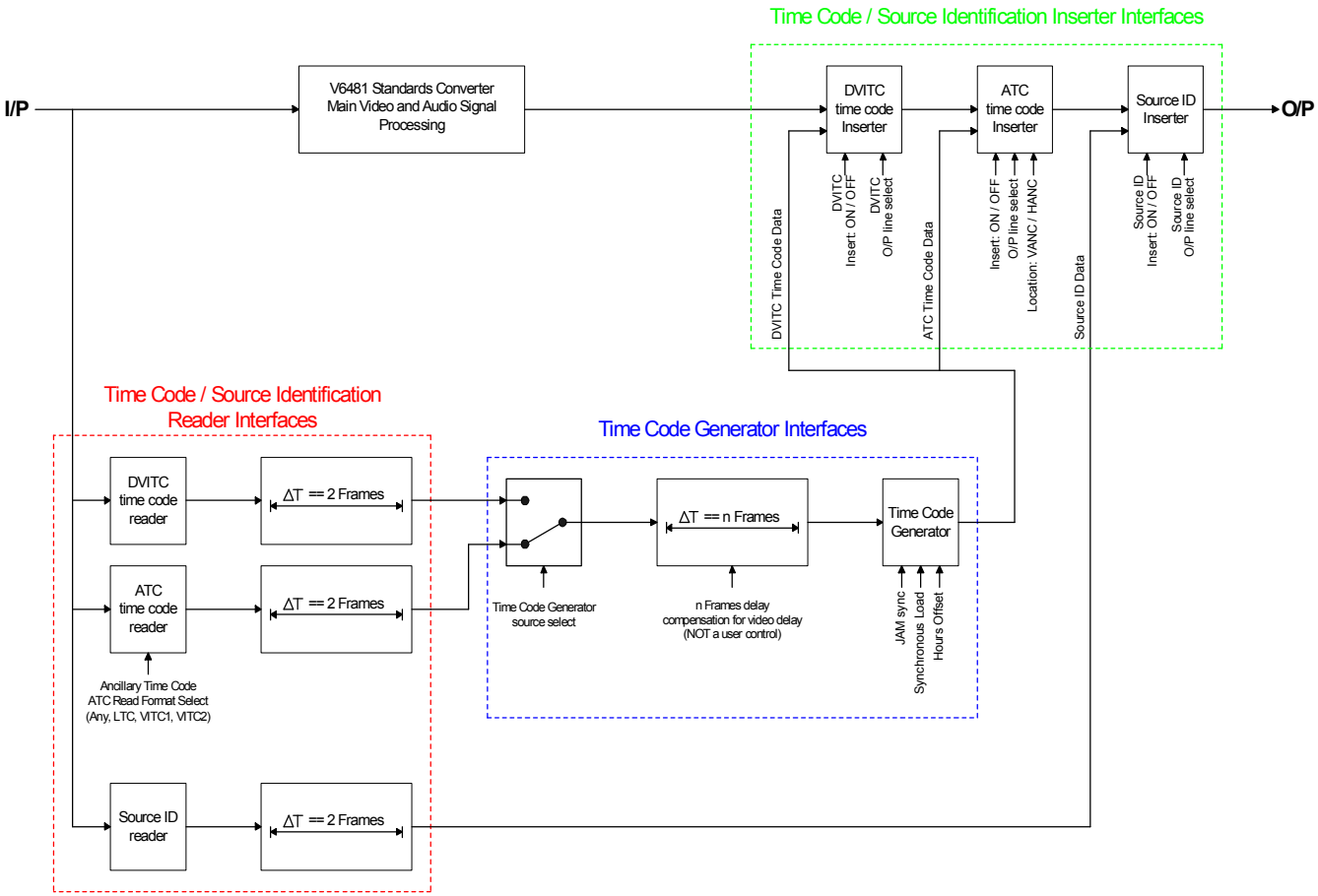
3.6.1 General

Cifer offers a number of time code and source identification processing features. The unit is able to read time code data from the input signal (Ancillary or DVITC coded) and fundamentally reproduce the same time code data at the output of the unit (Ancillary and/or DVITC coded). This transfer of time code data between the input and output of the unit may include a change in definition format (SD to HD or vica versa), change in format (1080i to 720p, etc) or very possibly a change in frame rate (50Hz to 59Hz, etc.).

The unit is also able to read source identification data from the input signal and fundamentaly reproduce the same source identification data at the output of the unit.

As shown in the diagram below, there are 3 main processing blocks:

1. Time code and source identification reader interfaces block.
2. Time code generator interfaces block.
3. Time code and source identification inserter interfaces block.



3.6.2 Time code and source ID reader interfaces block

The time code and source identification reader interfaces block contains three primary processing blocks: a DVITC time code reader, an Ancillary time code reader and a source identification reader.

The **DVITC time code reader** block reads and decodes DVITC time code from the input signal. It provides the following output signals for subsequent processing blocks:

Hours, minutes, seconds, frames data

32 user data bits

The **Ancillary Time Code (ATC) reader** block reads and decodes ATC time code from the input signal. It provides the following output signals for subsequent processing blocks:

Hours, minutes, seconds, frames data

32 user data bits

16 Distributed Binary Bits (DBB) data

There is one control available to the user via the front panel that modifies the operation of this block; this is the **ATC Read** control.

AUX DATA ATC Read

This allows the user to decide which type of encoded ATC time code to respond to and decode:

Any, **LTC**, **VITC1** or **VITC2**

The nominal position for this control is **Any**, and this should be the selection for the vast bulk of operational setups.

The **Source Identification (SID) reader** block reads and decodes source identification data from the input signal. It provides the following output signals for subsequent processing blocks:

Source identification data (15 characters)

3.6.3 Time code generator interfaces block

The time code generator interfaces block contains two primary processing blocks: a Time Code Generator (TCG) module and a Time Code Generator source selection switch.

The **Time Code Generator source selection switch** receives two sets of time code data (hours, minutes, seconds and frames) from the time code and source identification reader interfaces block. One set carries DVITC decoded time code data and the other carries ATC decoded time code data. The Time Code Generator source selection switch selects which set of time code data is passed on to the Time Code Generator module. This control (**TCG Src**) is available to the user via the front panel.

AUX DATA TCG Src

The two options for the setting of this control are:

TC ATC or **TC DVITC**

The **Time Code Generator module** is effectively a free running generator which is incremented at the output frame rate. To ensure that the input time code is reproduced at the output there is a synchronization process, known as Jam syncing, which effectively locks the output of time code generator to the selected input time code (DVITC or ATC). The Jam sync process is fully automatic (hidden from the user) and occurs momentarily at certain events. Examples of these events are when the input signal reappears after a period when there has been no input to the unit, when the front panel input source selection (input 1 > input 2) has changed, when there is a discontinuity in the incoming time code, etc. Although the Jam sync process is fully automatic, and does not require manual intervention from the user, there is also an optional manual Jam sync control available from the front panel.

AUX DATA TCG Jam

This is a momentary control. When a manual Jam sync is initiated from the front panel the text displayed on the front panel will momentarily toggle between **Off** and **Jam**, then return back to **Off**.

There are operational situations when a user may wish to offset the output time code with respect to the input time code by a number of integer hours. This feature is offered via a user adjustable front panel control (**TCG Ofst**).

AUX DATA TCG Ofst

This control is adjustable between -11 hours (**-11h**) and +12 hours (**+12h**) offset, in one hour increments. The nominal setting for this control is for there to be zero hours offset between the input and output time codes (**+0h**).

3.6.4 Time code and source ID inserter interfaces block

The time code and source identification inserter interfaces block contains three primary processing blocks: a DVITC time code inserter, an Ancillary time code inserter and a source identification inserter.

The **DVITC time code inserter** takes the raw time code data (hours, minutes, seconds, frames) from the Time Code Generator interfaces block, converts it into the appropriate DVITC coded signal and then adds it into the output signal path at the appropriate time in the vertical interval.

There are two controls available to the user via the front panel that modify the operation of this block; these are the **DVITCIns** and **DVITC Ln** controls.

AUX DATA DVITCIns

The two optional settings for this control are **DVITCOff** (Do not insert DVITC on the output signal) and **DVITC On** (Insert DVITC on the output signal).

AUX DATA DVITC Ln

The **DVITC Ln** control allows the user to decide into which line(s) in the vertical interval the DVITC time code data should be added. For each possible output standard there is a choice of 16 line pairs (one line in the first field, and the corresponding line in the second field). For example, the choice of line pairs for a 1080i50 output standard ranges from:

Ln 5/568 > **Ln13/576** (nominal setting) > **Ln20/583**

Please note: there are unique non-volatile storage locations for each possible output standard ie one location for 1080i50, one for 1080i59, one for 625i50, etc..

The **Ancillary Time Code (ATC) inserter** takes the raw time code data (hours, minutes, seconds, frames) from the Time Code Generator interfaces block, converts it into the appropriate ATC coded signal and then adds it into the output signal path at the appropriate time in the vertical interval.

There are three controls available to the user via the front panel that modify the operation of this block; these are the **ATC Ins**, **ATC Line** and **ATC Loc** controls.

AUX DATA ATC Ins

The two optional settings for this control are **ATC Off** (Do not insert ATC on the output signal) and **ATC On** (Insert ATC on the output signal).

AUX DATA ATC Line

The **ATC Line** control allows the user to decide into which line(s) in the vertical interval the ATC time code data should be added. For each possible output standard there is a choice of 16 line pairs (one line in the first field, and the corresponding line in the second field). For example, the choice of line pairs for a 1080i50 output standard ranges from:

Ln 5/568 > **Ln13/576** (nominal setting) > **Ln20/583**

Please note: there are unique non-volatile storage locations for each possible output standard ie one location for 1080i50, one for 1080i59, one for 625i50, etc..

AUX DATA ATC Loc

The two optional settings for this control are **ATC VANC** (Insert ATC in the VANC period of the output signal) and **ATC HANC** (Insert ATC in the HANC period of the output signal). The nominal setting for this control is **ATC VANC**.

The **Source Identification (SID) inserter** takes the raw source identification data (15 characters) from the time code and source identification reader interfaces block, converts it into the appropriate SID coded signal and then adds it into the output signal path at the appropriate time in the vertical interval.

There are two controls available to the user via the front panel that modify the operation of this block; these are the **SID Ins** and **SID Line** controls.

AUX DATA SID Ins

The two optional settings for this control are **SID Off** (Do not insert SID on the output

signal) and **SID On** (Insert SID on the output signal).

AUX DATA SID Line

The **SID Line** control allows the user to decide into which line(s) in the vertical interval the SID time code data should be added. For each possible output standard there is a choice of 16 line pairs (one line in the first field, and the corresponding line in the second field). For example, the choice of line pairs for a 1080i50 output standard ranges from:

Ln 5/568 > **Ln13/576** (nominal setting) > **Ln20/583**

Please note: there are unique non-volatile storage locations for each possible output standard ie one location for 1080i50, one for 1080i59, one for 625i50, etc..

The **Time Code on Output** control (**TCG Out**) allows the user to decide whether there should always be time code on the output of the unit, irrespective of if there is time code on the input signal, or not.

ENG'ING TCG Out

The two optional settings for this control are **From I/P** (Time Code inserted on the output of the unit **ONLY** if time code is present on the input to the unit) and **Always** (Time Code **ALWAYS** inserted on the output of the unit).

4 Calibration

This section describes how to calibrate the unit as it is done in the factory. The units do not contain any potentiometers, but like most equipment with analogue parts still needs to be calibrated. Normally this calibration is done in the factory and should not need to be repeated in the field but this section describes the procedure and is included for completeness.

High quality, calibrated test equipment should be used for this calibration. Note that it is not possible to return to the pre-calibration settings other than by making a note of the values and re-entering them.

4.1 Set-Up

There is a separate Main Level Menu for Calibration and this should be used throughout. The first sub-level menu is Cal Mode, which can be used to turn calibration ON:

```
CALIB      Cal Mode   Cal Off
                      Cal On
```

The calibration mode must be turned ON before any parameter can be adjusted. The calibration mode will be turned OFF in one of four ways:

- Manually on the **CALIB** : **Cal Mode** menu
- By going up to the Top Level Menu
- By re-powering the unit.
- By letting the display timeout and go to sleep mode.

When the calibration mode is ON then the unit will automatically set up the required conditions in the unit as you enter each sub-menu. For example, if you go into the CntrFreq sub-menu, the unit will automatically go into free run. For obvious reasons this should not be done on a unit that is being used On Air.

4.2 Free-Run Frequency

There is a voltage controlled crystal oscillator, which is usually locked to the external video reference or to the input video. However if there is no input or reference then it will free-run and this free running frequency should be set. The oscillator is not accurate enough to be used as a frequency reference, but nevertheless, should be set close to the ideal so that any succeeding SDI equipment will be able to lock to its output, and so that when in free run it will only drift slowly away from its starting reference.

To calibrate the frequency set the unit into Free Run by turning Cal Mode ON and selecting the CntrFreq sub-menu.

CALIB Cal Mode Cal On

Now compare the output picture movement on a monitor with an accurate external reference and adjust the frequency accordingly.

CALIB CntrFreq Range is -127 to +128

The setting is stored on the unit in non-volatile memory, and should not need regular adjustment.

5 Controls

The following tables show a complete list of all the parameters that can be controlled locally for the various configurations. Unless otherwise shown they can also be controlled over the DART remote control system. Not all menus are available at any one time, since they depend on module configurations and sometimes on the operating conditions.

The tables also show the full range of the controls and their ranges and normalised value, if appropriate. The normalised value or setting is shown by the '**n**'.

5.1 Video Processing – VIDEO

Main Menu	Sub Menu	Value		Comment	Notes
VIDEO	Source	I/P 1	n	Input Selection	
		I/P 2			
	O/P LStd	Vid I/P	n	Output line standard. **Vid I/P** selects the input line standard.	†
		525i			
		625i			
		1080i			
		720p			
	O/P FldR	Auto	n	Output field rate. **Auto** selects the input frame rate.	†
		59.94Hz			
		50Hz			
	A/R Up	16:9 ANA	n	Aspect ratio control for up-conversions. (SD > HD)	
		4:3 PB			
		14:9 PB			
		16:9 CC			
	A/R Down	4:3 ANA	n	Aspect ratio control for down-conversions. (HD > SD)	
		16:9 LB			
		14:9 LB			
		4:3 CC			
	AR SD>SD	[ ] > [ ]	n	Aspect ratio control for standard definition conversions. (SD > SD)	
		[ ]>16:9 CC			
		[ ]>14:9 PB			
		[ ]>16:9 CC			
		[ ] > [ ]			
		[ ]>16:9 LB			
		[ ]>14:9 LB			
		[ ]> 4:3 CC			
	SD Width	SDwd Dig	n	Selects whether SD aspect ratios should be based on analogue or digital blanking.	
		SDwd Ana			
	Norm	******			

† Greyed out options are available in the menu system but not supported at the time of print.

5.2 Video Proc Amp – PROC AMP

Main Menu	Sub Menu	Value		Comment	Notes
PROC AMP	V Gain	-6.02dB		Video Gain Control	
		⇓			
		-0.00dB	n		
		⇓			
		+6.01dB			
	C Gain	-6.02dB		Chroma Gain Control	
		⇓			
		-0.00dB	n		
		⇓			
		+6.01dB			
	Blk Lvl	-128		Black Level Control	
		⇓			
		+0	n		
		⇓			
		+127			
	Hue	-45.00°		Hue Control	
		⇓			
		+0.00°	n		
		⇓			
		+44.65°			
	Bypass	Byp Off	n	Proc Amp Bypass Off	
		Byp On		Proc Amp Bypass On	
	Dyn Rdn	DR On	n	Dynamic Rounding On	
		DR Off		Dynamic Rounding Off	
	Hrd Clip	HClp Off	n	Hard Clipping Off	
		HClp On		Hard Clipping On	
	Fade>Blk	F>B Off	n	Fade to Black Off	
		F>B On		Fade to Black On	
	Norm	******			

5.3 Audio Control - AUDIO

Main Menu	Sub Menu	Value		Comment	Notes
AUDIO	6302Data	6302 Off	n	Set this to '**6302 On**' to allow the V6302 to embed audio data into the output.	
		6302 On			
	Aud Grps	1 2 3 4		Number indicates group present – indicates group absent	s
		- 2 - 4			
		- - - -			
	V6302	V6302 ü		Ticked if V6302 module detected.	s
		V6302 X			
	Norm	******			

s These menu items are status only.

5.4 Timing Adjustments - TIMING

Main Menu	Sub Menu	Value		Comment	Notes
TIMING	H Timing	+0.00µs ⇓ +22.23µs	n	Horizontal offset relative to external reference (µs)	†
	V Timing	-256 ⇓ +0 ⇓ +255	n	Vertical offset relative to external reference (lines)	
	H Delay	+0 ⇓ +749	n	Horizontal offset relative to SDI input (µs)	‡
	V Delay	+0.00µs ⇓ +22.23µs	n	Vertical offset relative to SDI input (lines)	
	Ref Src	Auto	n	Timing reference source. **Auto** selects external reference if present, otherwise selects the SDI input.	
		Vid I/P			
		Ref I/P			
	RFL Mode	Min DLY	n	Reference fail mode.	
		Adj DLY			
	Ref Std	RF No I/P RF 625i50 RF 525i59 ...		Shows the standard of the external reference.	s
	Norm	******			

† Only available when timing is relative to an analogue reference. Range is dependent on output standard.
‡ Only available when timing is locked to the SDI input. Range is dependent on output standard.
n Default value.
s These menu items are status only.

5.5 Auxiliary Data – AUX DATA

Main Menu	Sub Menu	Value		Comment	Notes
AUX DATA	TCG Jam	Off	n	Time Code Generator manual Jam sync control	
		Jam		Momentary control:- forces Jam then returns to Off	
	TCG Ofst	+12h		O/P time code offset by +12 hours wrt I/P time code	
		⇓		Integer hours offset control between I/P and O/P TC	
		+0h	n	No offset between I/P and O/P time codes	
		⇓			
		-11h		O/P time code offset by -11 hours wrt I/P time code	
	TCG Load	Off	n	Time Code Generator manual Load control	
		Load		Momentary control:- forces Load then returns to Off	
	TCG Src	TC ATC	n	TCG source:- taken from ATC on input signal	
		TC DVITC		TCG source:- taken from DVITC on input signal	
	DVITCIns	DVITCOff	n	Do not insert DVITC on the output signal	
		DVITC On		Insert DVITC on the output signal	
	DVITC Ln	Ln20/583		< 1080i50 O/P	
		⇓		DVITC output line select	
		Ln13/576	n	< 1080i50 O/P	
		⇓			
		Ln 5/568		< 1080i50 O/P	
	ATC Read	AR Any	n	ATC reader:- read any form of ATC on I/P signal	
		AR LTC		ATC reader:- only detect LTC coded ATC on I/P	
		AR VITC1		ATC reader:- only detect VITC1 coded ATC on I/P	
		AR VITC2		ATC reader:- only detect VITC2 coded ATC on I/P	
	ATC Ins	ATC Off	n	Do not insert ATC on the output signal	
		ATC On		Insert ATC on the output signal	
	ATC Line	Ln20/583		< 1080i50 O/P	
		⇓		ATC output line select	
		Ln13/576	n	< 1080i50 O/P	
		⇓			
		Ln 5/568		< 1080i50 O/P	
	ATC Loc	ATC VANC	n	Location of ATC on output signal:- in VANC	
		ATC HANC		Location of ATC on output signal:- in HANC	
	SID Ins	SID Off	n	Do not insert Source ID on the output signal	
		SID On		Insert Source ID on the output signal	
	SID Line	Ln20/583		< 1080i50 O/P	
		⇓		SID output line select	
		Ln13/576	n	< 1080i50 O/P	
		⇓			
		Ln 5/568		< 1080i50 O/P	
	Norm	******			

5.6 System Status – STATUS

Main Menu	Sub Menu	Value		Comment	Notes
STATUS	Variant	V6481		HD / SD Outputs	s
		V6481SD		SD output only	
	Options	TC		Time code option fitted	
	V6302	V6302 ü		ü indicates that the V6302 unit has been detected	
		V6302 X			
	Aud Grps	1 2 3 4		Number indicates group present – indicates group absent	
		- 2 - 4			
		- - - -			
	Source	IP 1		Indicates the currently selected input.	
	I/P 1	IP 1 X		These indicate the presence of the two inputs.	
	I/P 2	IP 2 ü			
	I/P Std	I P 720p50		Format of the selected SDI input.	
	O/P Std	O P 525i59		Selected output SDI format.	
	Ref I/P	REF ü		Indicates presence of external video reference.	
	Ref Std	R F No I/P R F 625i50 R F 525i59 ...		Shows the standard of the external reference.	
	SC Temp	48.1°C		SC temperature.	
	MEC Temp	53°C		MEC temperature.	
	SC Fan	OK		V6481 Fan status	
	ME Fan	Fail		V6482 Fan status	
	TC Stat	TC ü		Indicates presence of selected time code source.	
	DVITC TC	--h--m--s--		DVITC Time Code from selected input video.	† s
	ATC TC	--h--m--s--		ATC Time Code from selected input video.	
	SID Text	No Sourc		DVITC Time Code read from input.	
		My SID Te...			
	Sub-Mod	M Fitted		Indicates that the video processor sub-module is fitted.	s

† When these items are selected, use the up and down buttons on the front panel to navigate the displayed text.
s These menu items are status only.

5.7 Engineering Menu – ENG'ING

Main Menu	Sub Menu	Value		Comment	Notes
ENG'ING	O/P EDH	EDH On	n	Enable/Disable EDH on SD outputs.	
		EDH Off			
	TCG Out	From I/P	n	Time code only inserted on output when it is detected on the input video.	
		Always		Time code always present on output video.	
	DefIpStd	720p59	n	Default input standard.	
	FanTest	Fan Both	n	Enables fan test on SC (V6481) and ME (V6482). **Note:** If a fan is tested on power up and fails, the Cifer unit will not start.	
		Fan SC			
		Fan ME			
		Fan none			
	H Res	H High	n	Horizontal resolution control **Note:** This only applies to down conversions	
		H Medium			
		H Low			
	V Res	V High	n	Vertical resolution control. **Note:** This only applies to down conversions.	
		V Medium			
		V Low			
	Mot Comp	MC On	n	Enables/Disables motion compensation when doing frame rate conversion.	
		MC Off			
	MEC Mode	0	n	Selects motion compensation algorithm. 0 – is the preferred mode in most cases.	
		1			
		2			
	Free-Run	Free Off	n	Forces the unit to ignore references and free-run.	
		Free On			
	Norm	******			

5.8 Calibration Menu – CALIB

Main Menu	Sub Menu	Value		Comment	Notes
CALIB	Cal Mode	Cal Off		Set to '**Cal On**' to allow adjustment of '**CntrFreq**'	
		Cal On			
	CntrFreq	Frq=-128		VCO centre frequency.	
		Frq= +0	n		
		Frq=+127			
	Norm	******			

5.9 Configuration Menu – CONFIG

Main Menu	Sub Menu	Value		Comment	Notes
CONFIG	Banner	On	n	When '**On**' enables warning message banners	
		Off			
	Sleep	zz 0 min ... zz 5 min ... zz 30 min	n	Length of time from last button push until front panel goes to sleep. When set to 0, the unit never sleeps.	
	LEDLevel	▓▓▓▓		Display brightness control.	
	Password	0			
	Variant	CIFER SD		Unit variant options.	s
	TestMode	Off	n	Puts unit into test mode.	
		On			
	Factory	Mode Off		Test purposes only.	s
	Norm	******			

5.10 System Version Information – VERSION

Main Menu	Sub Menu	Value		Comment	Notes
VERSION	PROM Ver	03.00		PROM stick version	†
	MEC Ver	2.20		V6482 software version	
	Soft Ver	05.01.00		Versions of software / firmware / hardware components.	‡
	Boot Ver	02.00.00			
	Strx Ver	1.4.00			
	FPGA Ver	01.02			
	CPLD Ver	00.01			
	Data Ver	29000002			‡
	PCB Ver	00.00			
	VPModule	MHD PROC			
	IOModule	STD [3]			

† These are the version numbers of the user upgradeable software in the V6481 and V6482.
'**PROM Ver**' relates to the physical memory stick plugged into the V6481 unit.
'**MEC Ver**' relates to the V6482 software upgradeable via USB.

‡ These are constituent parts of the PROM stick.

6 Appendix

6.1 Trouble Shooting Guide (Frequently Asked Questions)

This section is to be a help in solving some common difficulties. If there is no control from the front panel first check that the Rem/Local switch is set to *Local*.

Q:	My Cifer unit does not synchronise to the external reference.
A1:	Check whether the Front Panel Ref. LED is lit. This indicates the presence of an ext. reference.
A2:	Check whether the ext. reference input is selected. **`TIMING : Ref Src : Auto (or Ref IP)`**

Q:	The Proc Amp does not work.
A1:	Check whether it is set to Bypass. **`PROC AMP : Bypass : Byp Off`**

Q:	The display never goes to sleep.
A1:	Check whether the Sleep delay has been set to 0 Mins, which means stay awake.

6.2 Initialisation, Power On-Selftest & Error Messages

6.2.1 Board Initialisation Sequence

Every time a board goes through a power-on cycle, either by re-seating the board in the rack or by triggering the manual reset, a sequence of initialisation and self-test events is being carried out by the on-board microcontroller.

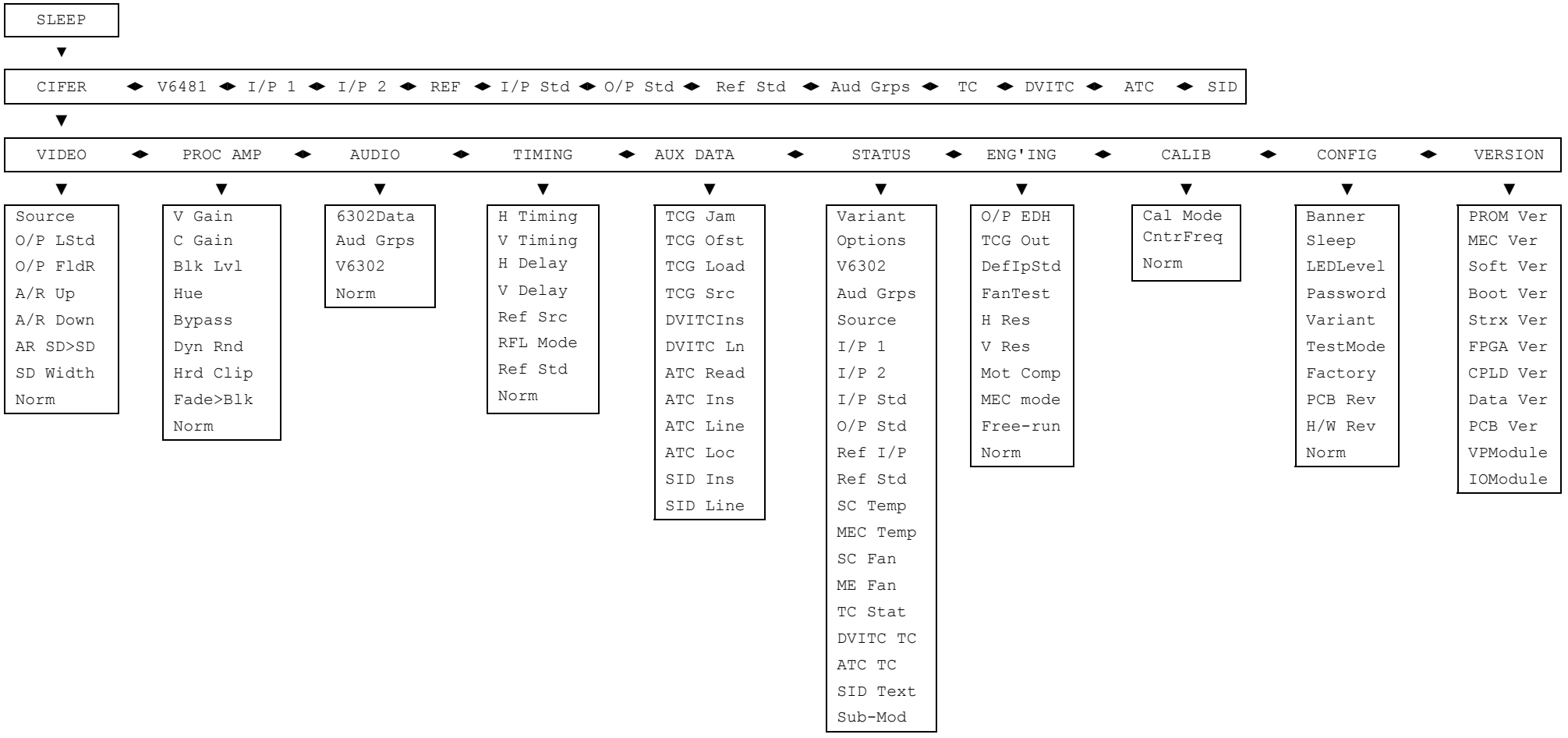
If anything goes wrong, an error message is shown on the front panel display and program execution halts. The following table shows the error messages and their meaning:

Flash upgrading	ERROR 01	Flash erasing failed
	ERROR 02	Flash programming failed
	ERROR 03	Main program checksum error after programming
	ERROR 04	Bootloader checksum error after programming
	ERROR 05	No program loaded and no valid upgrade in Flash Stick
	ERROR 06	Bootloader upgrade required but no valid bootloader upgrade in Flash Stick
FPGA Load	ERROR 07	STATUS stayed low after CONFIG pulsed low
	ERROR 08	DONE stayed high after CONFIG pulsed low
	ERROR 09	STATUS went low during configuration
	ERROR 10	DONE stayed low after configuration
Local EEPROM	ERROR 11	Error writing to local EEPROM
	ERROR 12	Error reading from EEPROM
	ERROR 13	Initialising EEPROM to default data
	ERROR 14	Initialising parameters to default data
Debug Port	ERROR 15	Receive buffer overflow
	ERROR 16	Receive overrun
	ERROR 17	Receive framing error
	ERROR 18	Receive parity error

6.3 Menu Structure

The following page summarizes the menu structure on the Cifer module.

Please note that the presence of some sub-menus depend on the factory configuration of your module. In other words, if an option is not fitted, the entire sub-menu belonging to it will not appear in the menu structure.


SLEEP
CIFER
V6481
I/P 1
I/P 2
REF
I/P Std
O/P Std
Ref Std
Aud Grps
TC
DVITC
ATC
SID
VIDEO
PROC AMP
AUDIO
TIMING
AUX DATA
STATUS
ENG'ING
CALIB
CONFIG
VERSION
Source
O/P LStd
O/P FldR
A/R Up
A/R Down
AR SD>SD
SD Width
Norm
V Gain
C Gain
Blk Lvl
Hue
Bypass
Dyn Rnd
Hrd Clip
Fade>Blk
Norm
6302Data
Aud Grps
V6302
Norm
H Timing
V Timing
H Delay
V Delay
Ref Src
RFL Mode
Ref Std
Norm
TCG Jam
TCG Ofst
TCG Load
TCG Src
DVITCIns
DVITC Ln
ATC Read
ATC Ins
ATC Line
ATC Loc
SID Ins
SID Line
Variant
Options
V6302
Aud Grps
Source
I/P 1
I/P 2
I/P Std
O/P Std
Ref I/P
Ref Std
SC Temp
MEC Temp
SC Fan
ME Fan
TC Stat
DVITC TC
ATC TC
SID Text
Sub-Mod
O/P EDH
TCG Out
DefIpStd
FanTest
H Res
V Res
Mot Comp
MEC mode
Free-run
Norm
Cal Mode
CntrFreq
Norm
Banner
Sleep
LEDLevel
Password
Variant
TestMode
Factory
PCB Rev
H/W Rev
Norm
PROM Ver
MEC Ver
Soft Ver
Boot Ver
Strx Ver
FPGA Ver
CPLD Ver
Data Ver
PCB Ver
VPModule
IOModule